

Model Name: GA-H81M-HD3

Revision 1.01

SHEET

TITLE

01	COVER SHEET
02	BOM & PCB MODIFY HISTORY
03	BLOCK DIAGRAM
04	CPU_LGA1150-A
05	CPU_LGA1150-B
06	CPU_LGA1150-C
07	DDR III CHANNEL A
08	DDR III CHANNEL B
09	PCH_FDI,DMI,USB,PCIE,NVRAM
10	PCH_DP,CLK BUFFER
11	PCH_HOST,SATA,PCI
12	PCH_GPIO,CTRL,AUDIO
13	PCH_PWR,GND
14	PCI EXPRESS X16 SLOT
15	PCI EXPRESS X1 SLOT
16	PCI SLOT 1,2
17	ITE 8620 LPC IO
18	COM,LPT,KB_MS
19	HWM,FAN CTRL,OV,-PROCHOT
20	DUAL BIOS
21	R_USB30,FP,FUSB,SPK,SATALED
22	CODEC ALC892
23	REAR AUDIO JACK
24	REALTEK RTL8111F
25	DISCRETE POWER
26	ATX
27	VCORE ISL95812_1

SHEET

TITLE

28	VCORE ISL95812_2
29	RT8120_DDR POWER
30	DVI
31	ITE IT8892E
32	USB3 VL805
33	HDMI/DP
34	F_USB30

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Cover Sheet

Size Custom	Document Number GA-H81M-HD3	Rev 1.01
Date: Friday, September 13, 2013	Sheet 1 of 33	

Model Name: GA-H81M-HD3

Revision 1.01

Component value change history

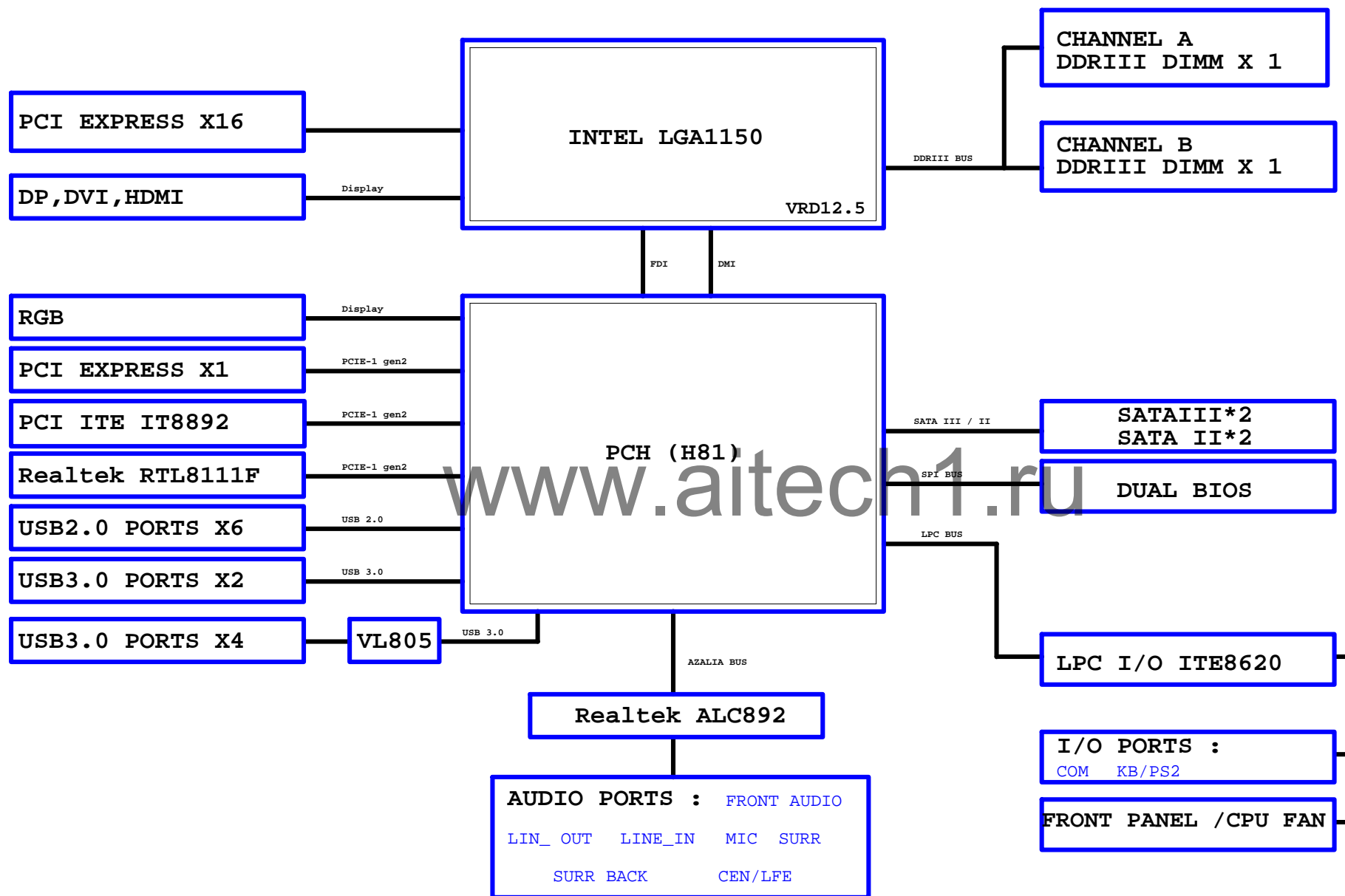
2013/04/22

[illegible]

Circuit or PCB layout change

[illegible]

BLOCK DIAGRAM



[illegible]

Legend:

- Red: FDI signals
- Blue: Other signals
- Green: Power/Ground signals

Connections:

Signal	Pin	Signal	Pin
FDI_CS	D16	FDI_CS	D16
FDI_INT	D18	FDI_INT	D18
FDI_RCOMP	R4	FDI_RCOMP	R4
FDI_TXN0	B14	FDI_TXN0	B14
FDI_TXP0	A14	FDI_TXP0	A14
FDI_TXN1	C13	FDI_TXN1	C13
FDI_TXP1	B13	FDI_TXP1	B13

Other connections (Blue lines):

- VCCIOA_L to WR23 (24.9/4/1)
- N_DP_CLK to U5
- N_DP_CLK to U6
- EDP_DISP_UTIL to E16
- RSVD_TP to K11
- RSVD_TP to J12

Power/Ground connections (Green lines):

- DP_TX0 to F17
- DP_TX0 to F17
- DP_TX0 to F18
- DP_TX0 to F18
- DP_TX0 to G19
- DP_TX0 to G19
- DP_TX0 to F20
- DP_TX0 to F20
- DP_TX0 to G20
- DP_TX0 to G20
- DP_TX0 to D19
- DP_TX0 to D19
- DP_TX0 to E19
- DP_TX0 to E19
- DP_TX0 to C20
- DP_TX0 to C20
- DP_TX0 to D20
- DP_TX0 to D20
- DP_TX0 to D21
- DP_TX0 to D21
- DP_TX0 to E21
- DP_TX0 to E21
- DP_TX0 to C22
- DP_TX0 to C22
- DP_TX0 to D22
- DP_TX0 to D22
- DP_TX0 to B15
- DP_TX0 to B15
- DP_TX0 to C15
- DP_TX0 to C15
- DP_TX0 to A16
- DP_TX0 to A16
- DP_TX0 to B16
- DP_TX0 to B16
- DP_TX0 to B17
- DP_TX0 to B17
- DP_TX0 to C17
- DP_TX0 to C17
- DP_TX0 to A18
- DP_TX0 to A18
- DP_TX0 to B18
- DP_TX0 to B18

CPU-SK/1150/S/GF

FDI:12/4/5/4/12(breakout min 6/4/4/4/6)
Impedance=85 +- 17.5%

FDI_TXP0_11 >>> FDI_TXP0[0..1] 9

FDI_TXN0_11 >>> FDI_TXN0[0..1] 9

PCIEX16:16/5/5/16(breakout min 10/4/4/4/10)									
Impedance=80 +/- 17.5%									
LGA1150C									
PA EXP_RXP0	E15	PEG_RXP0	TXP0	A12	PA EXP_TXP0				
PA EXP_RXN0	F15	PEG_RXN0	TXN0	B12	PA EXP_TXN0				
PA EXP_RXP1	D14	PEG_RXP1	TXP1	B11	PA EXP_TXP1				
PA EXP_RXN1	E14	PEG_RXN1	TXN1	C11	PA EXP_TXN1				
PA EXP_RXP2	E13	PEG_RXP2	TXP2	C10	PA EXP_TXP2				
PA EXP_RXN2	F13	PEG_RXN2	TXN2	D10	PA EXP_TXN2				
PA EXP_RXP3	D12	PEG_RXP3	TXP3	B9	PA EXP_TXP3				
PA EXP_RXN3	E12	PEG_RXN3	TXN3	C9	PA EXP_TXN3				
PA EXP_RXP4	E11	PEG_RXP4	TXP4	C8	PA EXP_TXP4				
PA EXP_RXN4	F11	PEG_RXN4	TXN4	D8	PA EXP_TXN4				
PA EXP_RXP5	F10	PEG_RXP5	TXP5	B7	PA EXP_TXP5				
PA EXP_RXN5	G10	PEG_RXN5	TXN5	C7	PA EXP_TXN5				
PA EXP_RXP6	F9	PEG_RXP6	TXP6	A6	PA EXP_TXP6				
PA EXP_RXN6	F9	PEG_RXN6	TXN6	B6	PA EXP_TXN6				
PA EXP_RXP7	F8	PEG_RXP7	TXP7	B5	PA EXP_TXP7				
PA EXP_RXN7	G8	PEG_RXN7	TXN7	C5	PA EXP_TXN7				
PA EXP_RXP8	D3	PEG_RXP8	TXP8	E1	PA EXP_TXP8				
PA EXP_RXN8	D4	PEG_RXN8	TXN8	E2	PA EXP_TXN8				
PA EXP_RXP9	E4	PEG_RXP9	TXP9	F2	PA EXP_TXP9				
PA EXP_RXN9	E5	PEG_RXN9	TXN9	G3	PA EXP_TXN9				
PA EXP_RXP10	F5	PEG_RXP10	TXP10	F1	PA EXP_TXP10				
PA EXP_RXN10	F6	PEG_RXN10	TXN10	G2	PA EXP_TXN10				
PA EXP_RXP11	G4	PEG_RXP11	TXP11	H2	PA EXP_TXP11				
PA EXP_RXN11	G5	PEG_RXN11	TXN11	H3	PA EXP_TXN11				
PA EXP_RXP12	H5	PEG_RXP12	TXP12	J1	PA EXP_TXP12				
PA EXP_RXN12	H6	PEG_RXN12	TXN12	J2	PA EXP_TXN12				
PA EXP_RXP13	J4	PEG_RXP13	TXP13	K2	PA EXP_TXP13				
PA EXP_RXN13	J5	PEG_RXN13	TXN13	K3	PA EXP_TXN13				
PA EXP_RXP14	K5	PEG_RXP14	TXP14	M2	PA EXP_TXP14				
PA EXP_RXN14	K6	PEG_RXN14	TXN14	J3	PA EXP_TXN14				
PA EXP_RXP15	L4	PEG_RXP15	TXP15	L1	PA EXP_TXP15				
PA EXP_RXN15	L5	PEG_RXN15	TXN15	L2	PA EXP_TXN15				
PA EXP_RXP16	U3	PEG_RXP16	TXP16						
PA EXP_RXN16	U4	PEG_RXN16	TXN16						
PA EXP_RXP17	T3	PEG_RXP17	TXP17						
PA EXP_RXN17	U1	PEG_RXN17	TXN17						
PA EXP_RXP18	W2	PEG_RXP18	TXP18						
PA EXP_RXN18	W3	PEG_RXN18	TXN18						
PA EXP_RXP19	W4	PEG_RXP19	TXP19						
PA EXP_RXN19	W5	PEG_RXN19	TXN19						
PA EXP_RXP20	W6	PEG_RXP20	TXP20						
PA EXP_RXN20	W7	PEG_RXN20	TXN20						
PA EXP_RXP21	W8	PEG_RXP21	TXP21						
PA EXP_RXN21	W9	PEG_RXN21	TXN21						
PA EXP_RXP22	W10	PEG_RXP22	TXP22						
PA EXP_RXN22	W11	PEG_RXN22	TXN22						
PA EXP_RXP23	W12	PEG_RXP23	TXP23						
PA EXP_RXN23	W13	PEG_RXN23	TXN23						
PA EXP_RXP24	W14	PEG_RXP24	TXP24						

1.1V分壓

VCC3

WR26
2K41/X

A_CPURST

WR31
1K41/X

BC102
1n4/XTR/50V/K

1.1V

For IT8620 Ctrl

CPU_VTT_OR

WR3	90.9/4/1/X	PVIDSLCK
WR2	115/4/1	PVIDSOUT
WR4	75/4/1	-PVIDALRT

CPU_VTT_OR

WR14	51/4/1/X	A TMS
WR16	51/4/1/X	A TDO
WR17	51/4/1/X	A TDI
WR30	51/4/1	A -HPRDY
WR11	51/4/1	A TCK
WR9	51/4/1	A -TRST

Figure 10: Example of a 100MHz DDR2 memory controller configuration. The diagram shows a DDR2 memory controller with various pins and their connections. The top row shows pins WR55 (1K4/I/X) and 1K4/I/X. The second row shows A_THRMTRIP connected to WR8 (1K4/I) and VCC1_0. The third row shows A_PWR_DEBUG connected to WR34 (150/I/4) and VCC1_0. The fourth row shows A_TESTLOW_1 connected to WR33 (10K/I/4/X). The fifth row shows A_TESTLOW_2 connected to WR21 (8.2K/I/X) and 3VDD. The sixth row shows A_DBR connected to WR20 (0/I/X) and N_S_NY. The bottom section lists several DDR2 memory banks and their connections: A_DDR_COMP0 (WR28, 100/I/4), A_DDR_COMP1 (WR19, 76/I/4), A_DDR_COMP2 (WR22, 100/I/4), A_TESTLOW_1 (WR18, 49.9/I/4), A_TESTLOW_2 (WR12, 49.9/I/4), and A_HSW_CFG_RCOMP (WR24, 49.9/I/4).

DDR_15V

WR62
100k/1

WR60
100k/1

A_SM_VREF

WC3
0.1u/4/X7R/16V/K

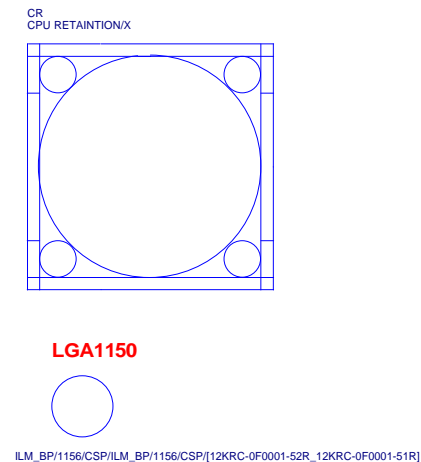
LGA1150 (A)



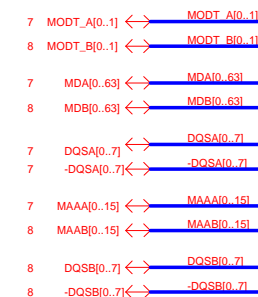
LGA1150 (B)



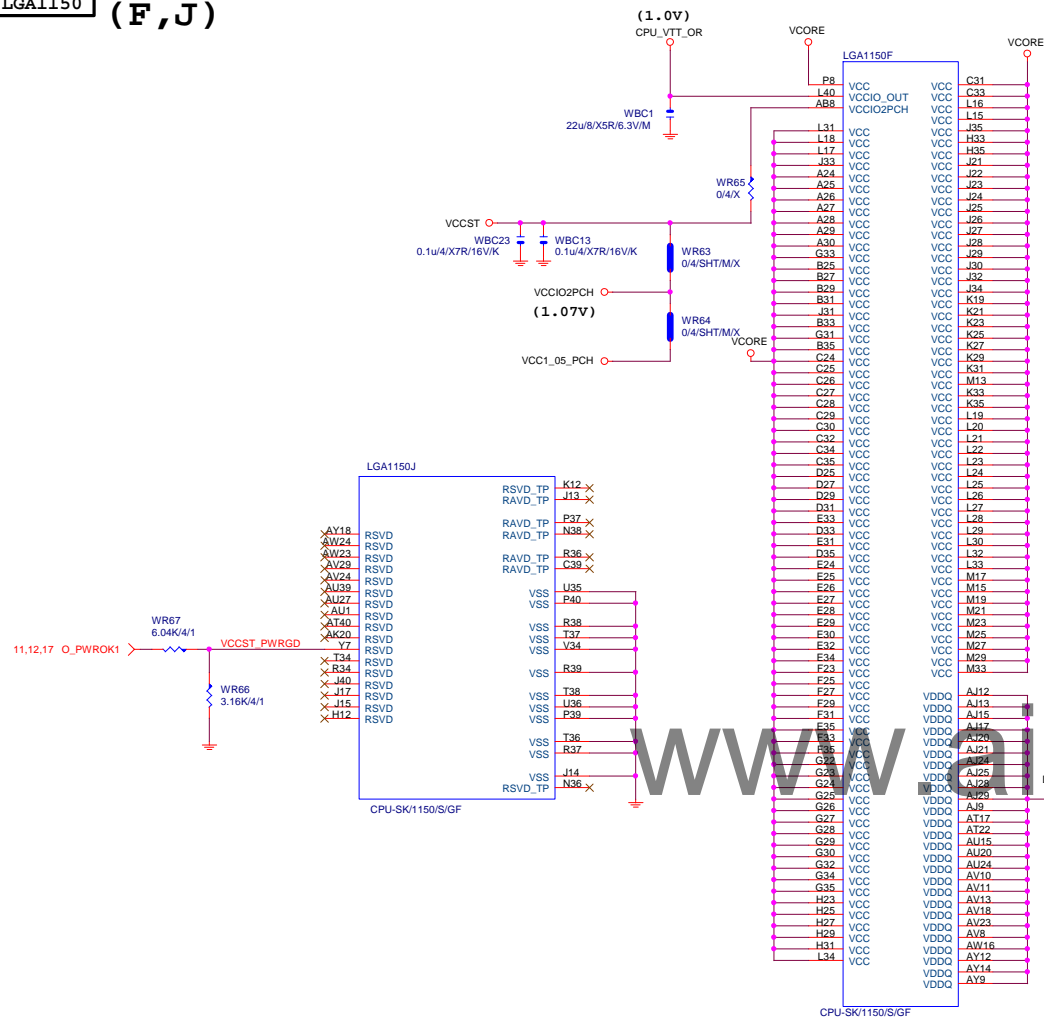
LGA1150 (CR)



DDR BUS



LGA1150 (F, J)

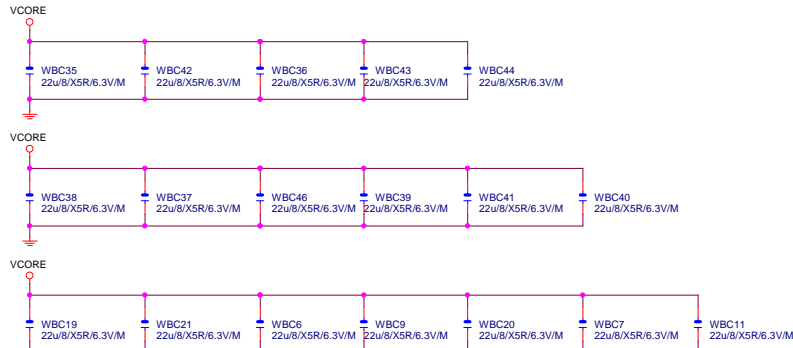


LGA1155 (G,H,I)



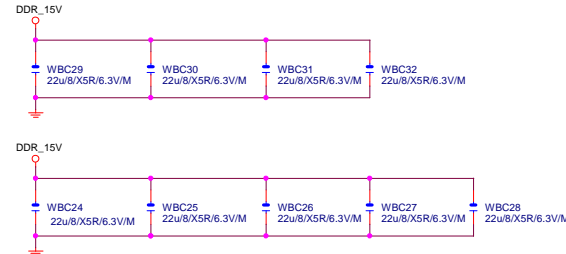
VCore CAP

(X18)



DDR CAP

(x9)



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Title	CPU11 GA1150-C
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Size	Document Number	Rev
Custom	GA-H81M-HD3	1.0

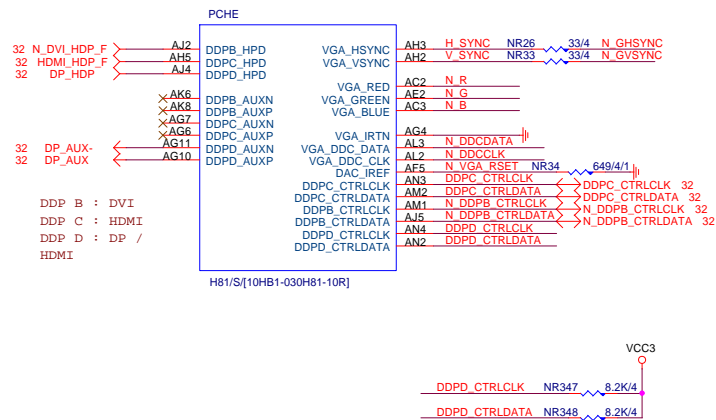
Date:	Friday, September 13, 2013	Sheet	6	of	33
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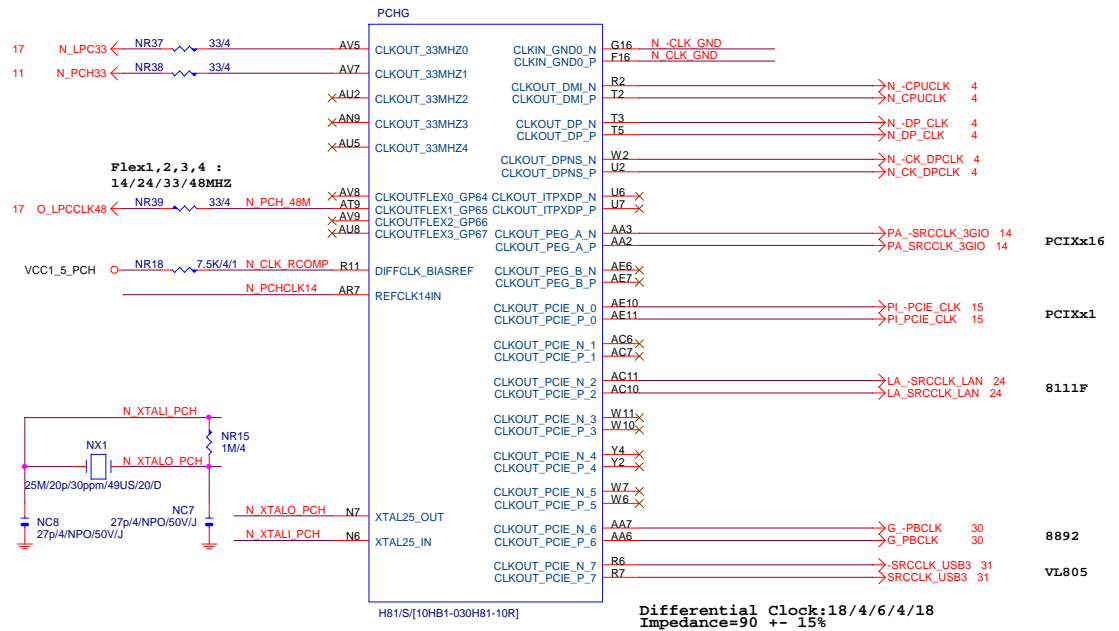
DIMM1 CHB

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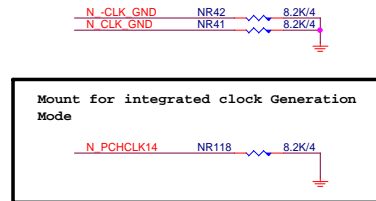
PCH (E)



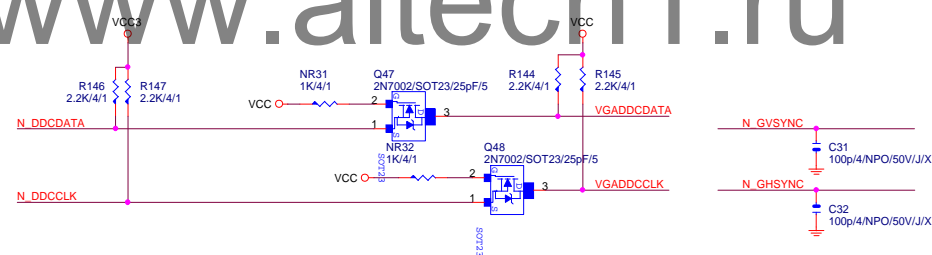
PCH (G)



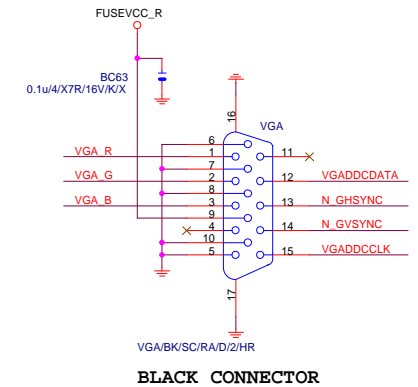
PCH CLK PD



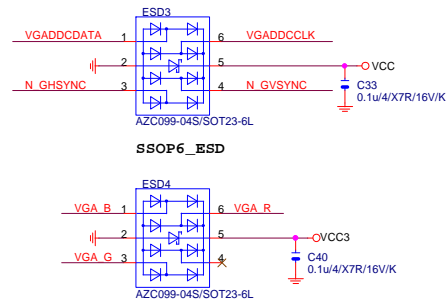
VGA DDC



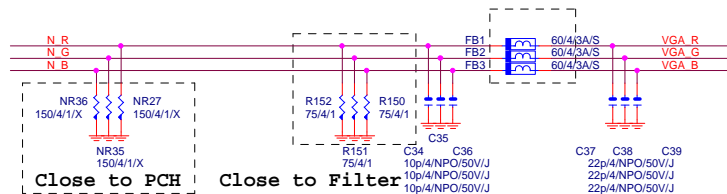
VGA CONNECTOR



VGA ESD

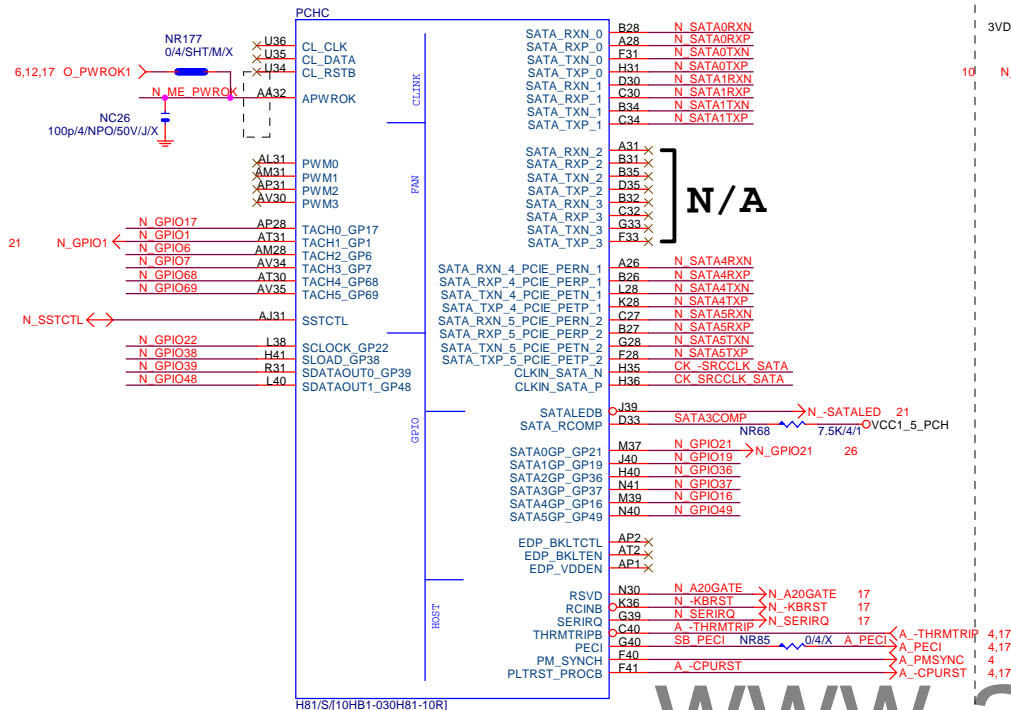


VGA DDC

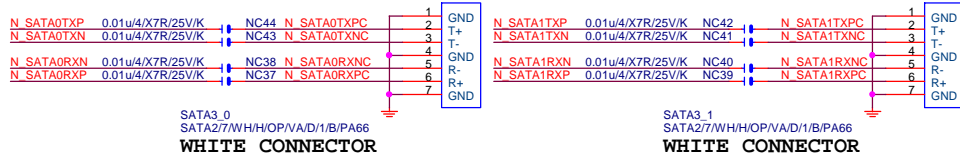


(C)

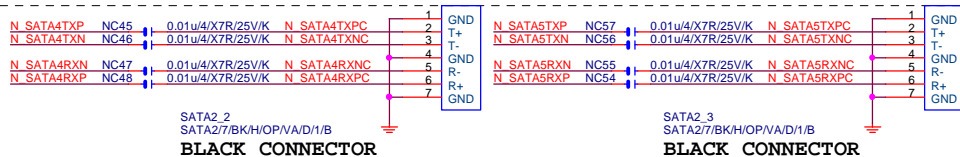
```
SATA3 : 20/7.5/4.5/7.5/20 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
SATA2 : 15/7.5/4.5/7.5/15 (breakout min 8/4/4/4/8)
Impedance=90 +- 17.5%
```



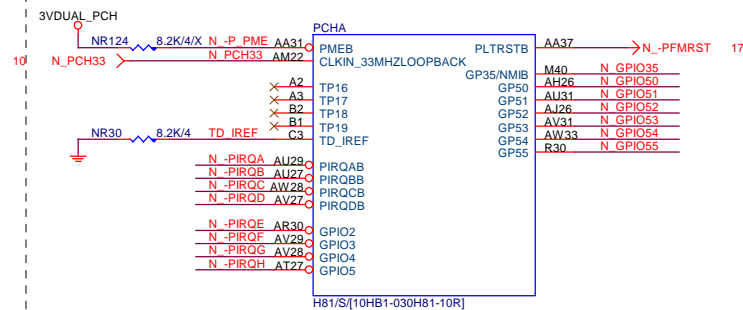
SATA CONNECTOR



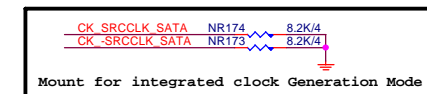
```
** Z87/H87 Port 4&5 SATA3.0
** B85 Port 4&5 SATA2.0
```



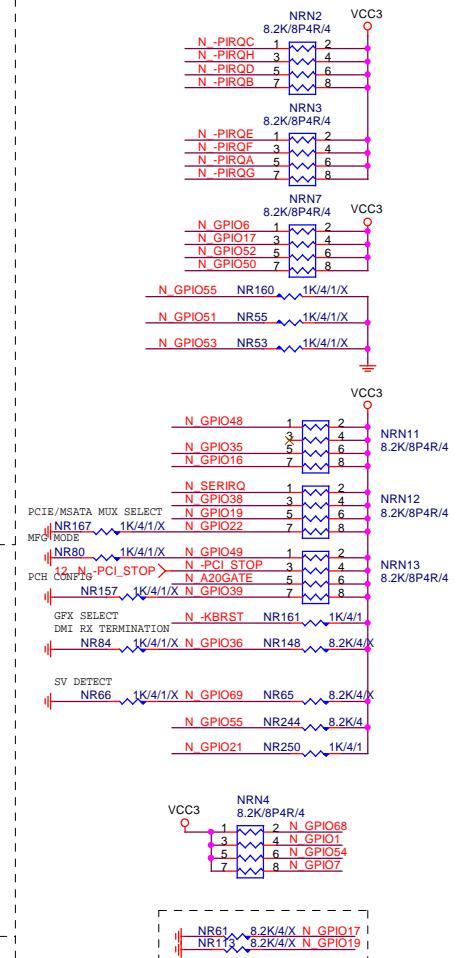
PCH (A)



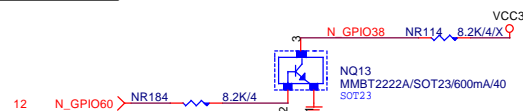
PCH	CLK	PD
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PCH	PU/PD
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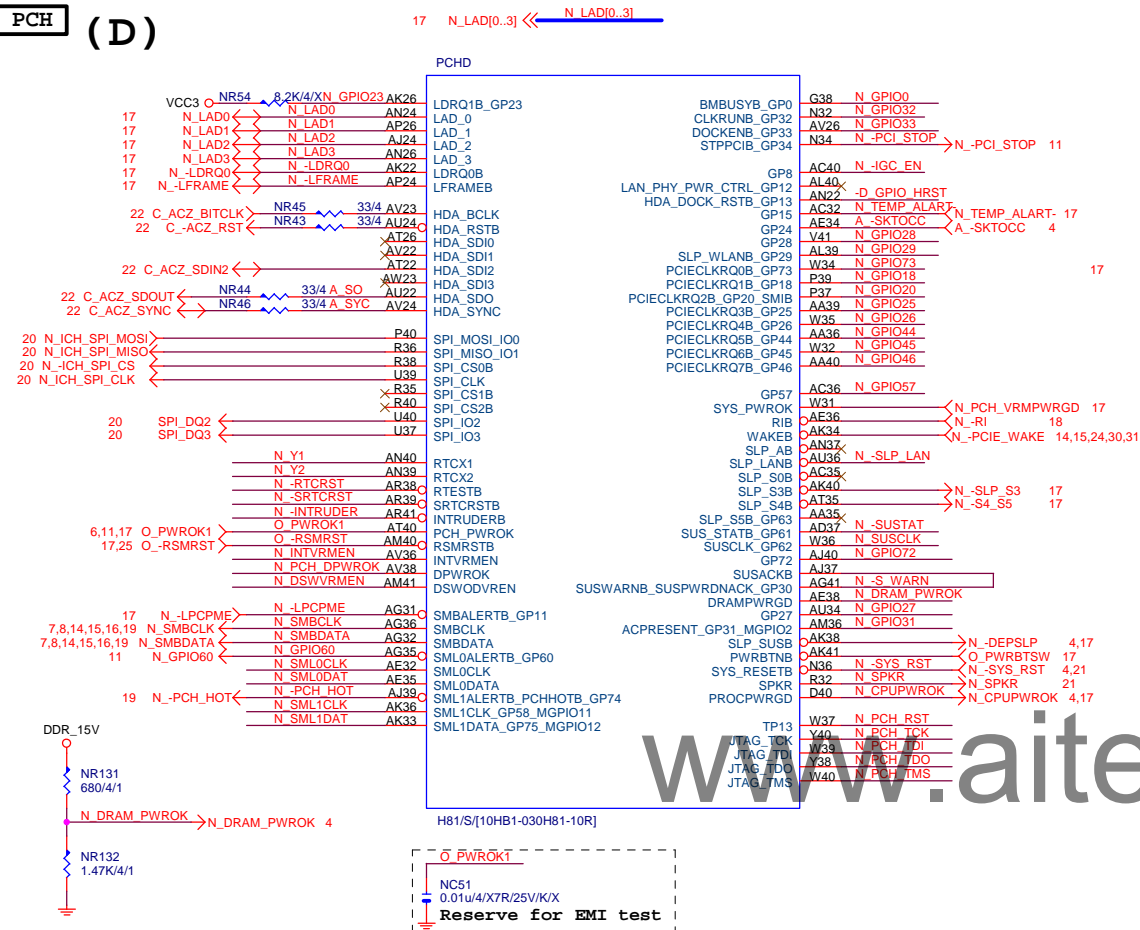
GPIO38 Ctrl



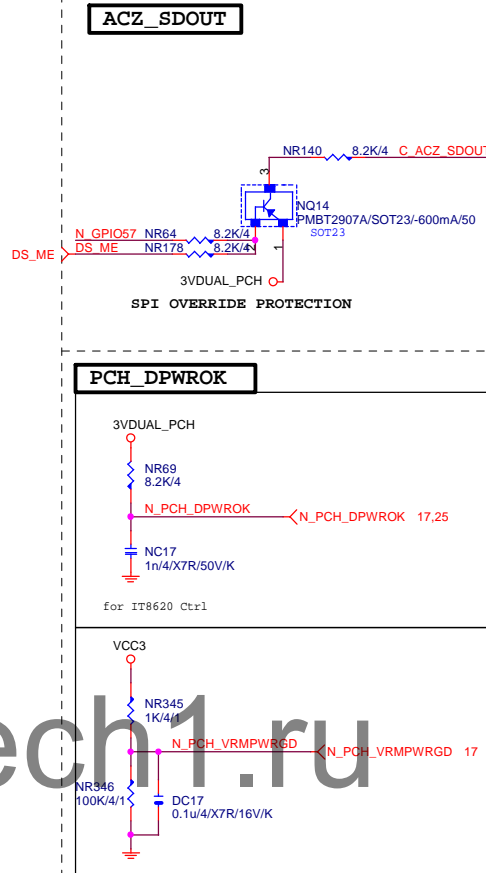
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Title			
PCH HOST , SATA, PCI			
Size	Document Number	Rev	
Custom	GA-H81M-HD3	1.0	
Date:	Friday, September 13, 2013	Sheet	11 of 33

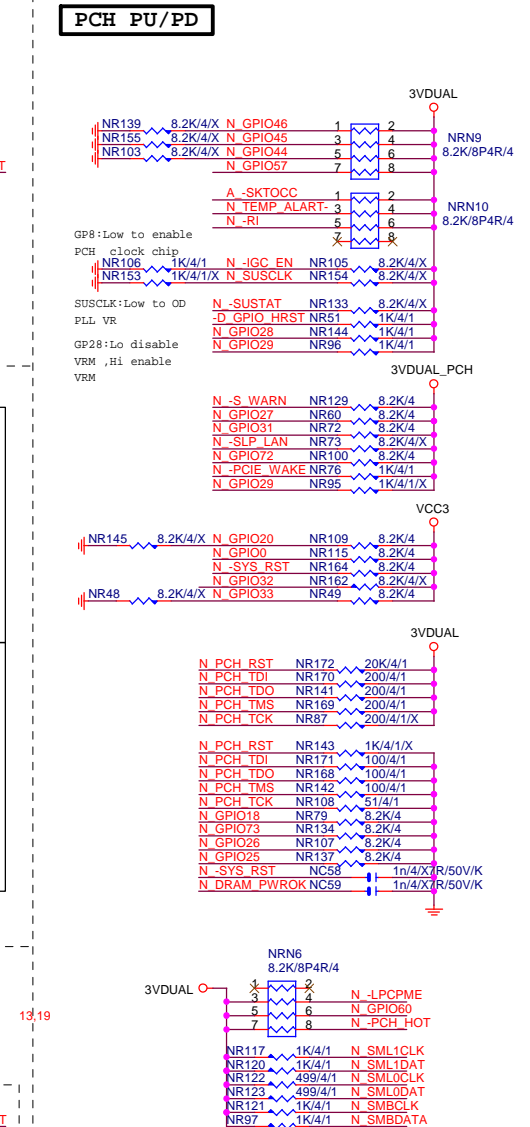
(D)



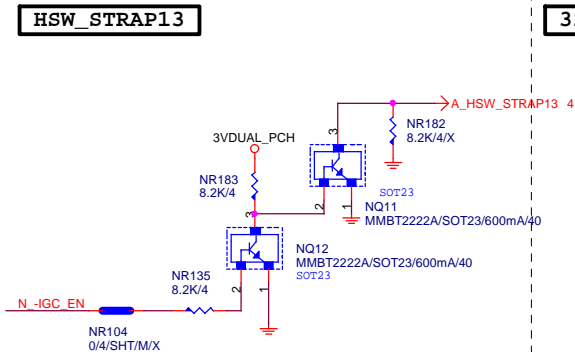
ACZ_SDOUT



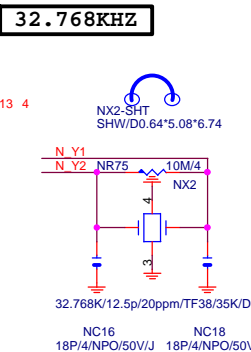
PCH	PU/PD
-----	-------



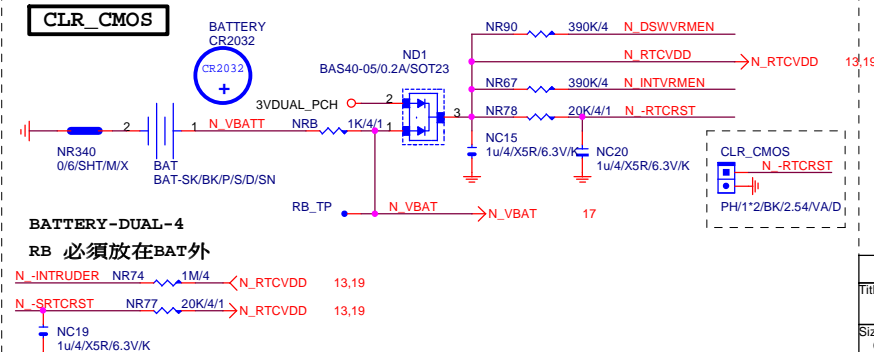
HSW_STRAP13



32.768KHZ



CLR_CMOS



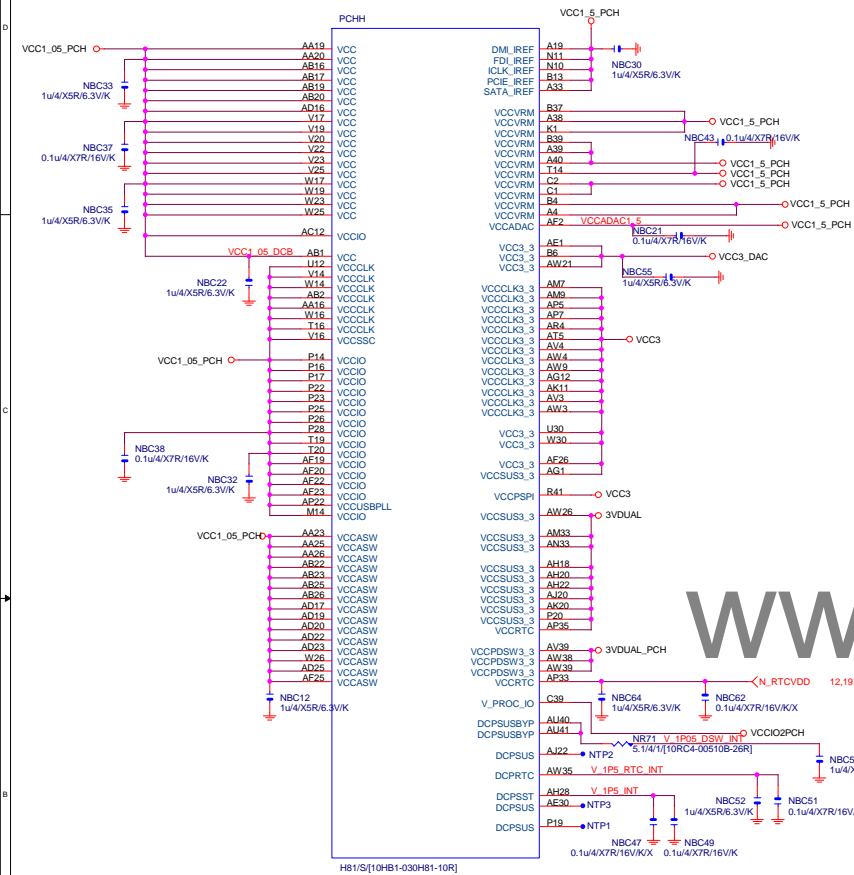
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PCH GPIO , CTRL , AUDIO

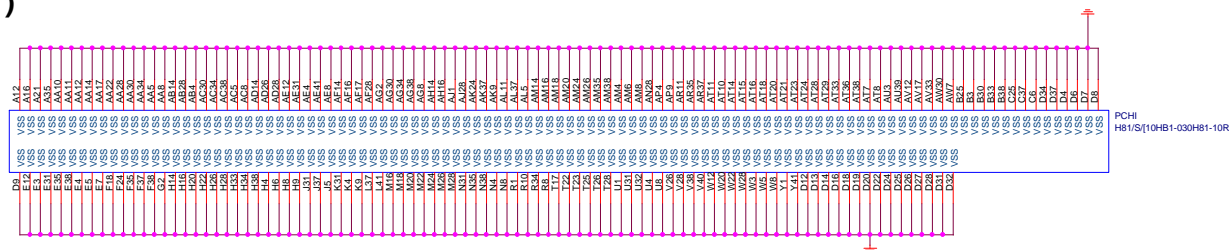
per **GA-H81M-HD3**

Rev	1.01
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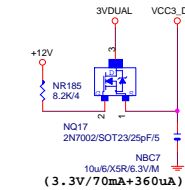
PCH (H)



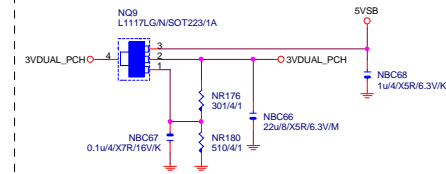
PCH (I)



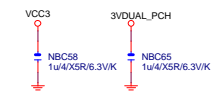
VCC3_DAC



3VDUAL_PCH



SHT PWR



CAP

(3.3V) (X6)

(1.05V) (x5)

(1.05V)(x6)

(1.05V)(x2) (3.3V)(x2)

(1.05V) (x10)

VCC1.5_PCH

NBC29 10uW/X5R/6.3V/M

NBC30 10uW/X5R/6.3V/M

NBC50 10uW/X5R/6.3V/M

NBC53 10uW/X5R/6.3V/M

NBC19 1u4/X5R/6.3V/K

NBC23 0.1u4/X7R/16V/K

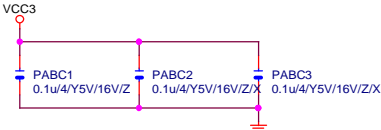
NBC28 1u4/X5R/6.3V/K

NBC44 1u4/X5R/6.3V/K

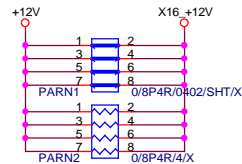
NBC5 0.1u4/X7R/16V/K

NBC48 1u4/X5R/6.3V/K

PCIEX16 CAP



PCIEX16 PROTECT SHT

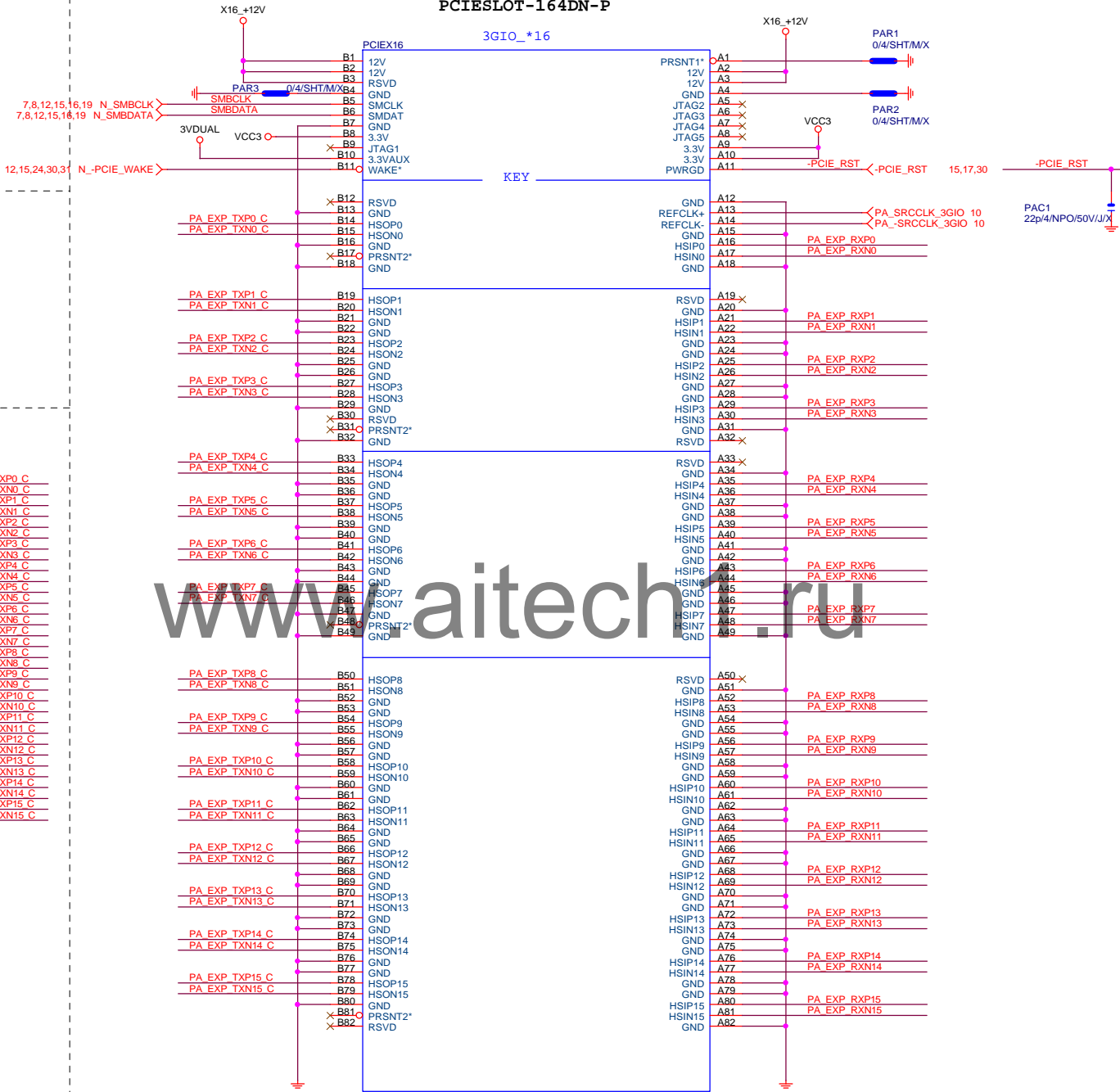


PCIEX16 AC CAP

PA EXP TXP0	PAC5	0.22u4/X5R/6.3V/K	PA EXP TXP0 C
PA EXP TXN0	PAC4	0.22u4/X5R/6.3V/K	PA EXP TXN0 C
PA EXP TXP1	PAC6	0.22u4/X5R/6.3V/K	PA EXP TXP1 C
PA EXP TXN1	PAC7	0.22u4/X5R/6.3V/K	PA EXP TXN1 C
PA EXP TXP2	PAC8	0.22u4/X5R/6.3V/K	PA EXP TXP2 C
PA EXP TXN2	PAC9	0.22u4/X5R/6.3V/K	PA EXP TXN2 C
PA EXP TXP3	PAC10	0.22u4/X5R/6.3V/K	PA EXP TXP3 C
PA EXP TXN3	PAC11	0.22u4/X5R/6.3V/K	PA EXP TXN3 C
PA EXP TXP4	PAC12	0.22u4/X5R/6.3V/K	PA EXP TXP4 C
PA EXP TXN4	PAC13	0.22u4/X5R/6.3V/K	PA EXP TXN4 C
PA EXP TXP5	PAC14	0.22u4/X5R/6.3V/K	PA EXP TXP5 C
PA EXP TXN5	PAC15	0.22u4/X5R/6.3V/K	PA EXP TXN5 C
PA EXP TXP6	PAC16	0.22u4/X5R/6.3V/K	PA EXP TXP6 C
PA EXP TXN6	PAC17	0.22u4/X5R/6.3V/K	PA EXP TXN6 C
PA EXP TXP7	PAC18	0.22u4/X5R/6.3V/K	PA EXP TXP7 C
PA EXP TXN7	PAC19	0.22u4/X5R/6.3V/K	PA EXP TXN7 C
PA EXP TXP8	PAC20	0.22u4/X5R/6.3V/K	PA EXP TXP8 C
PA EXP TXN8	PAC21	0.22u4/X5R/6.3V/K	PA EXP TXN8 C
PA EXP TXP9	PAC22	0.22u4/X5R/6.3V/K	PA EXP TXP9 C
PA EXP TXN9	PAC23	0.22u4/X5R/6.3V/K	PA EXP TXN9 C
PA EXP TXP10	PAC24	0.22u4/X5R/6.3V/K	PA EXP TXP10 C
PA EXP TXN10	PAC25	0.22u4/X5R/6.3V/K	PA EXP TXN10 C
PA EXP TXP11	PAC26	0.22u4/X5R/6.3V/K	PA EXP TXP11 C
PA EXP TXN11	PAC27	0.22u4/X5R/6.3V/K	PA EXP TXN11 C
PA EXP TXP12	PAC28	0.22u4/X5R/6.3V/K	PA EXP TXP12 C
PA EXP TXN12	PAC29	0.22u4/X5R/6.3V/K	PA EXP TXN12 C
PA EXP TXP13	PAC30	0.22u4/X5R/6.3V/K	PA EXP TXP13 C
PA EXP TXN13	PAC31	0.22u4/X5R/6.3V/K	PA EXP TXN13 C
PA EXP TXP14	PAC32	0.22u4/X5R/6.3V/K	PA EXP TXP14 C
PA EXP TXN14	PAC33	0.22u4/X5R/6.3V/K	PA EXP TXN14 C
PA EXP TXP15	PAC34	0.22u4/X5R/6.3V/K	PA EXP TXP15 C
PA EXP TXN15	PAC35	0.22u4/X5R/6.3V/K	PA EXP TXN15 C

PA EXP RXP0.[15] >>>PA_EXP_RXP[0..15] 4
PA EXP RXN0.[15] >>>PA_EXP_RXN[0..15] 4
PA EXP TXP0.[15] >>>PA_EXP_TXP[0..15] 4
PA EXP TXN0.[15] >>>PA_EXP_TXN[0..15] 4

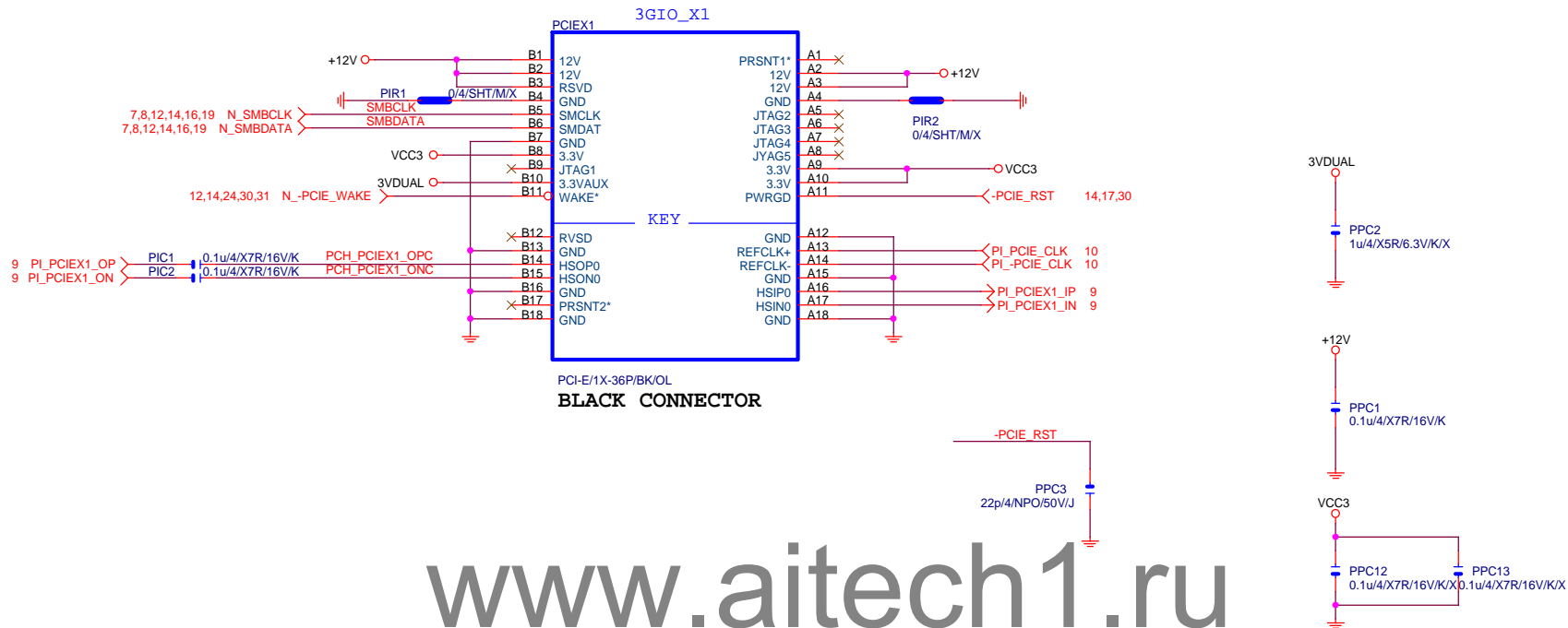
PCIEX16 SLOT



BLACK CONNECTOR

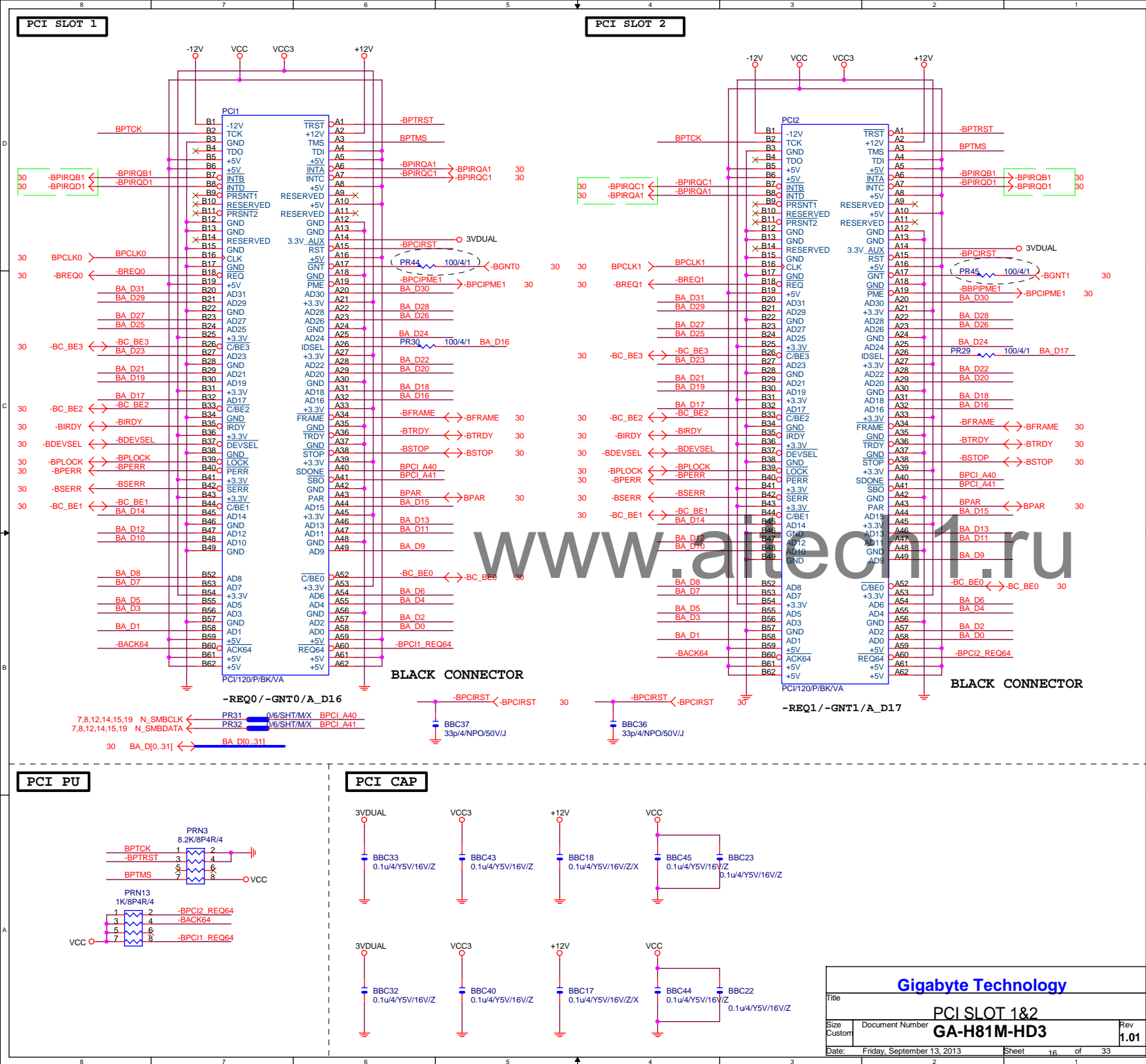
Gigabyte Technology		
Title		
PCI EXPRESS * 16		
Size	Document Number	Rev
Custom	GA-H81M-HD3	1.01
Date:	Friday, September 13, 2013	Sheet 14 of 33
		2

PCIEX1 SLOT

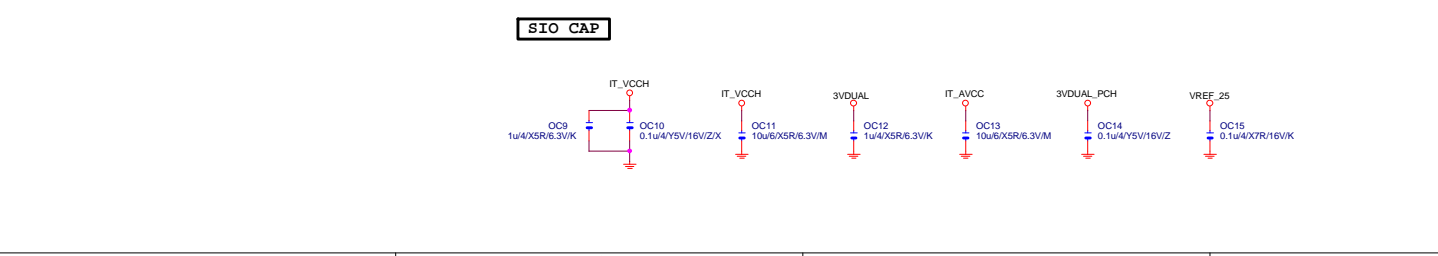
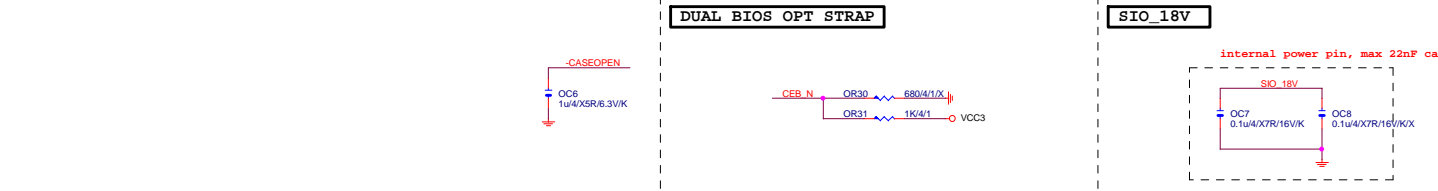
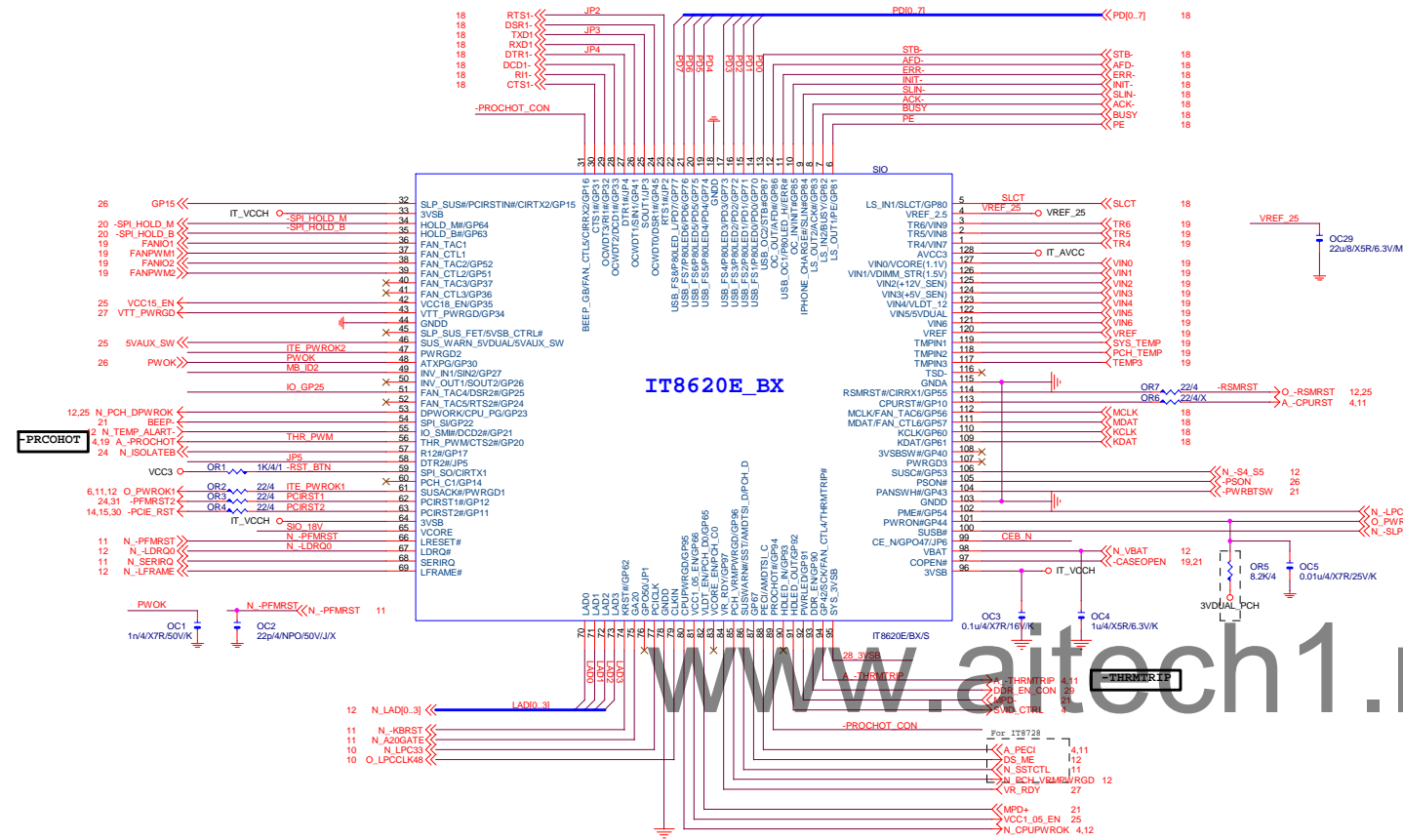


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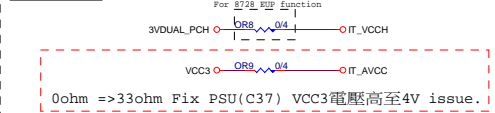
Gigabyte Technology			
Title			
PCI EXPRESS X 1 PORT			
Size	Document Number	Rev	
Custom		1.01	
Date:	Friday, September 13, 2013	Sheet	15 of 33



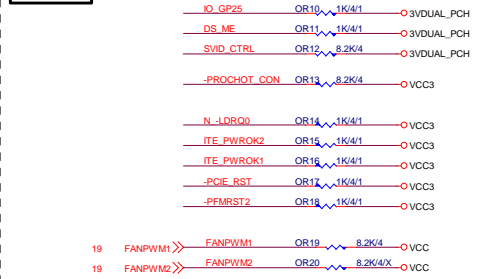
SIO IT8620



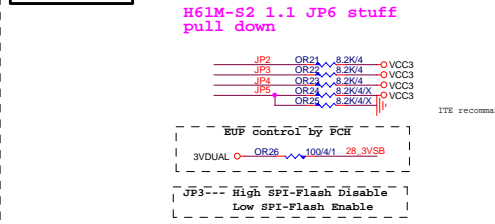
Power SHT



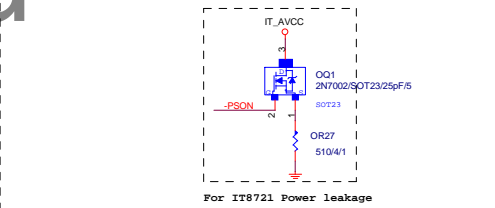
SIO PU



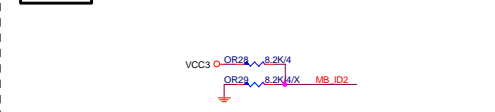
SIO STRAP



Power leakage

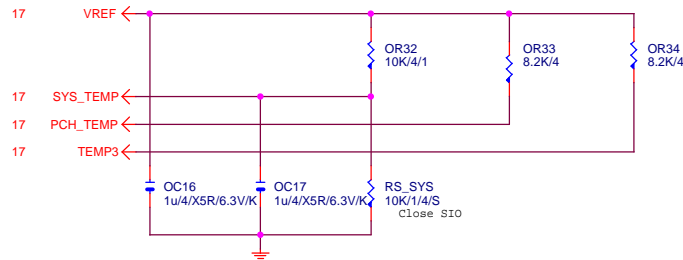


MB ID

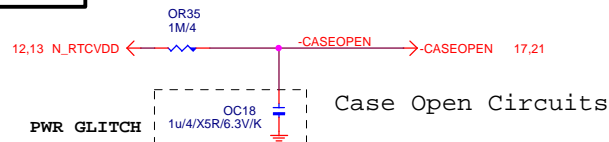


Gigabyte Technology			
SIO IT8620			
GA-H81M-HD3	Rev	1.01	
Date:	Friday, September 13, 2013	Sheet	17 of 33

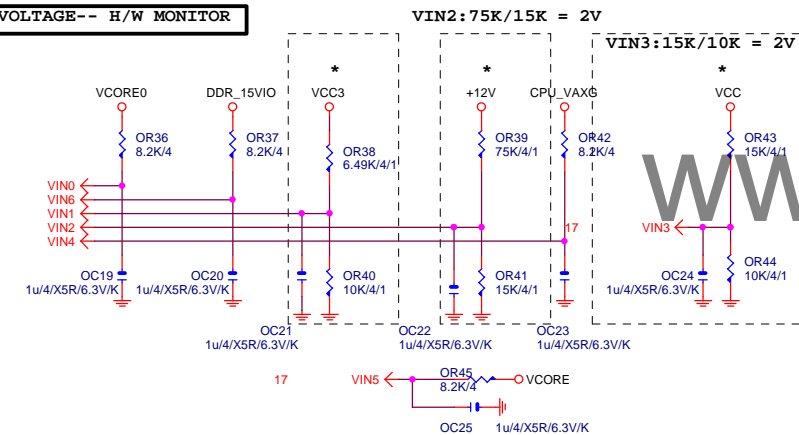
TEMP H/W MONITOR



CASE OPEN

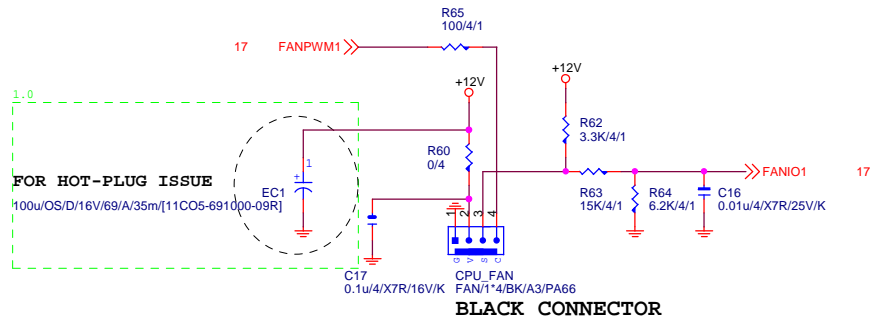


VOLTAGE-- H/W MONITOR

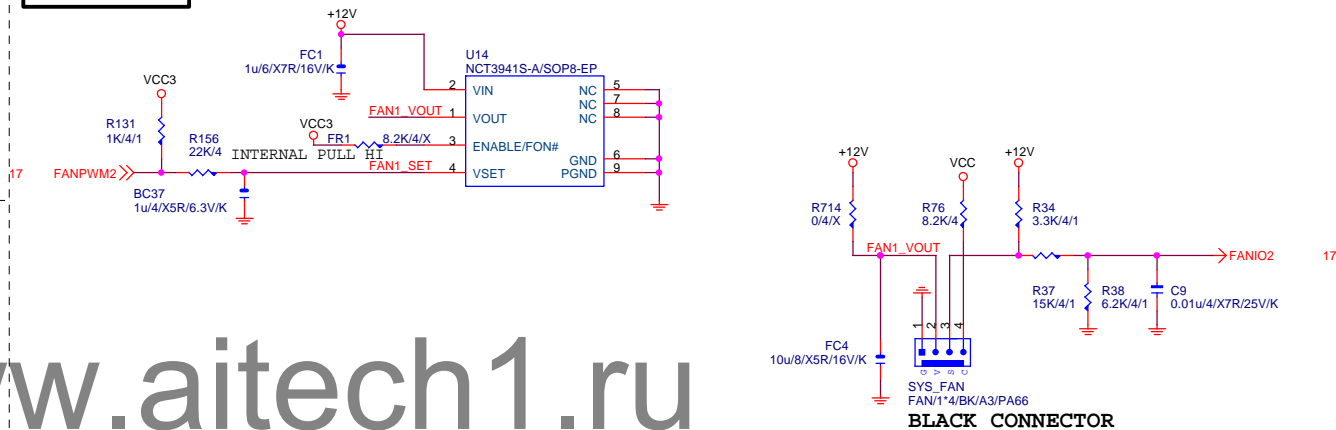


RS1、RS2、RS3 CLOSE CPU
VR MOSFET

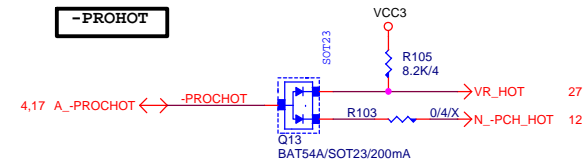
CPU SMART FAN



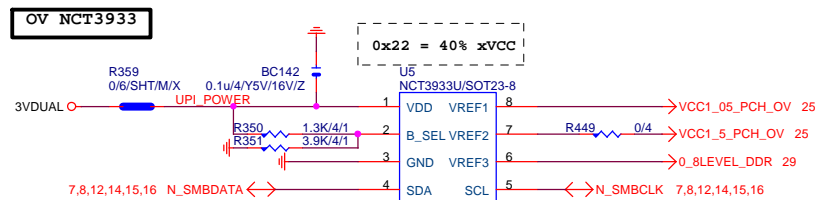
SYS SMART FAN



-PROHOT

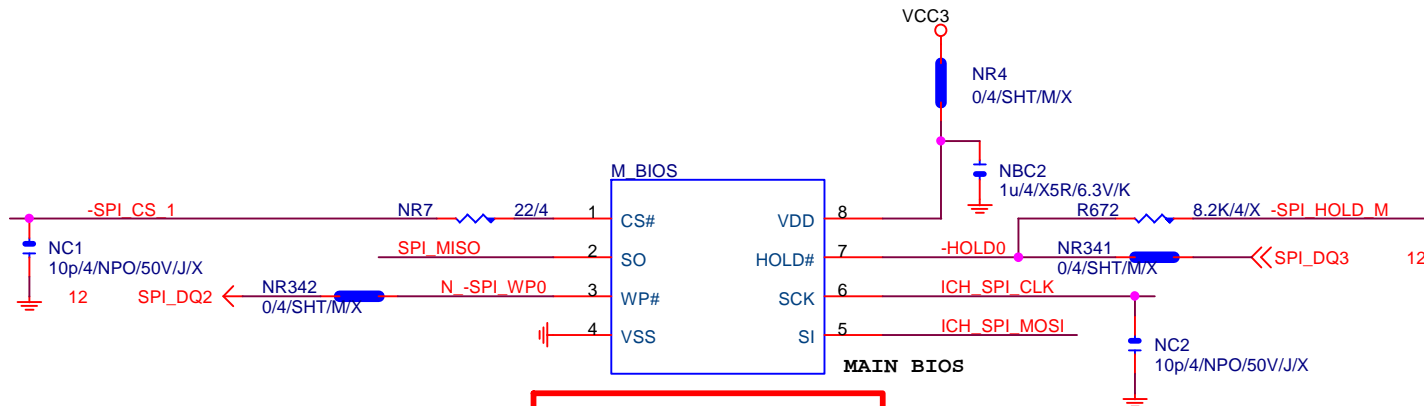


接pwm feedback pin

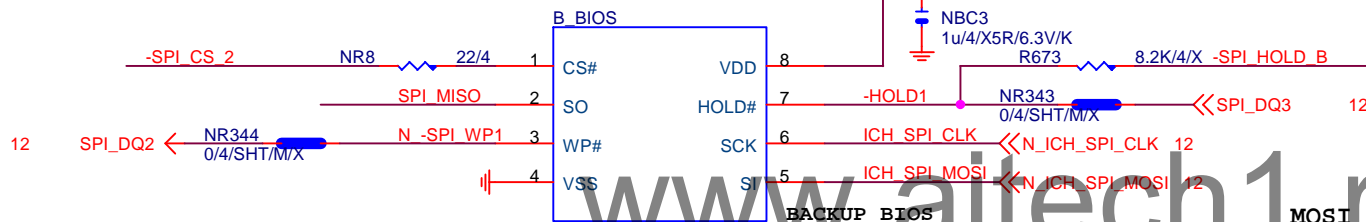


Gigabyte Technology

Title				Rev 1.01
HWM,FAN CTRL,OV				
Size Custom	Document Number GA-H81M-HD3			
Date:	Friday, September 13, 2013	Sheet	19 of 33	



64M/Q/SPI/SO8/S/[10HP4-112564-30R]

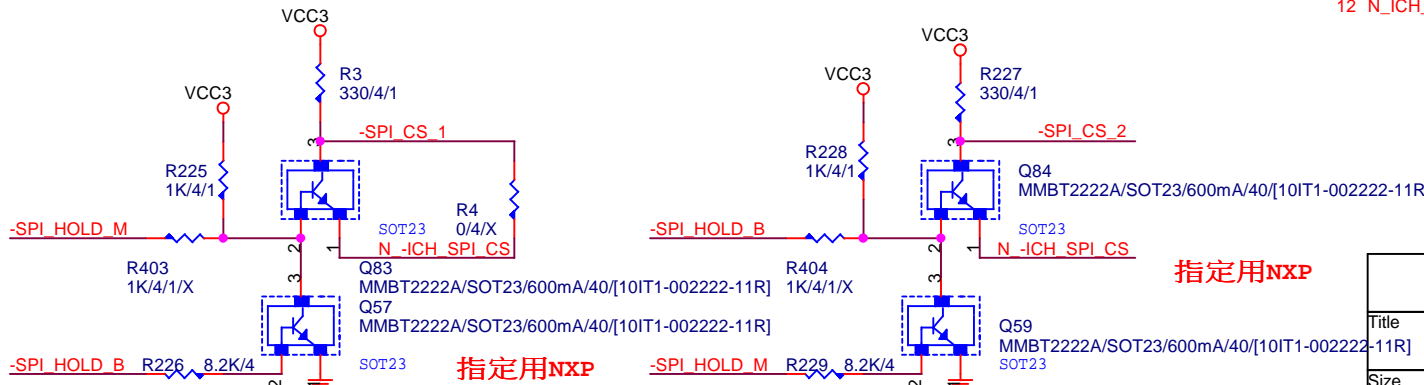
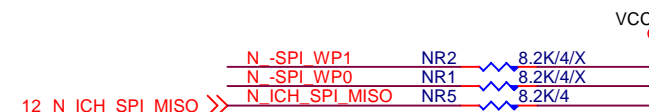
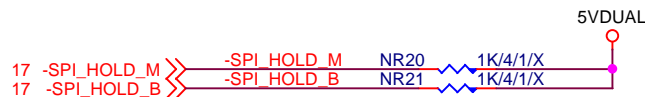
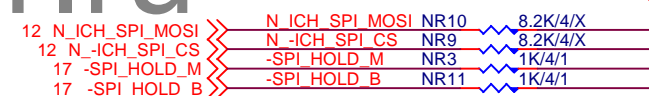


64M/Q/SPI/SO8/S/[10HP4-112564-30R]

BOOT DEVICE	GNT0	GNT1
LPC	0	0
PCI	0	1
NAND	1	0
SPI	1	1

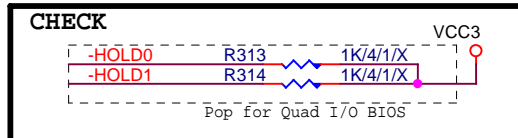
1 means floating
0 means PD 1K

MOSI For DMI RX Termination Voltage



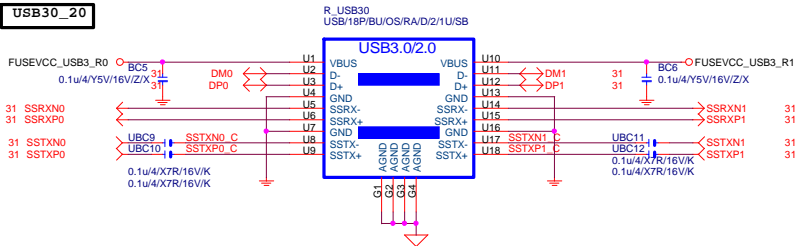
指定用NXP

指定用NXP

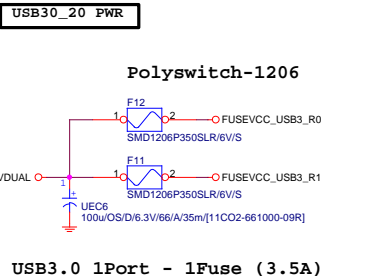


Gigabyte Technology		
DUAL BIOS		
Title	Document Number	Rev
	GA-H81M-HD3	1.01
Date:	Friday, September 13, 2013	Sheet 20 of 33

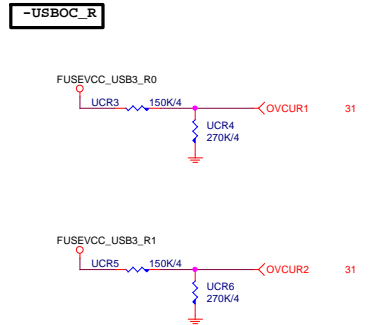
USB30_20



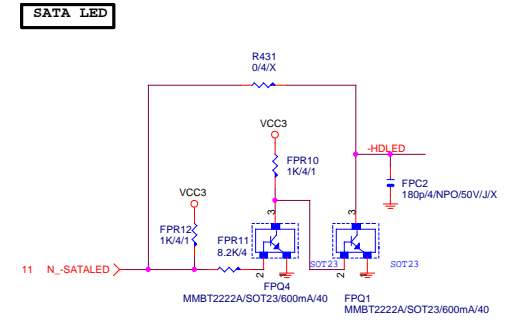
USB30_20 PWR



-USBOC_R

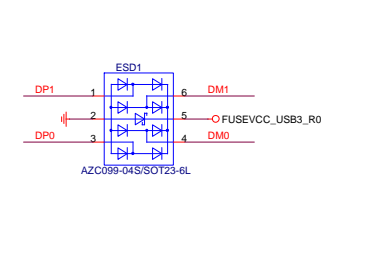
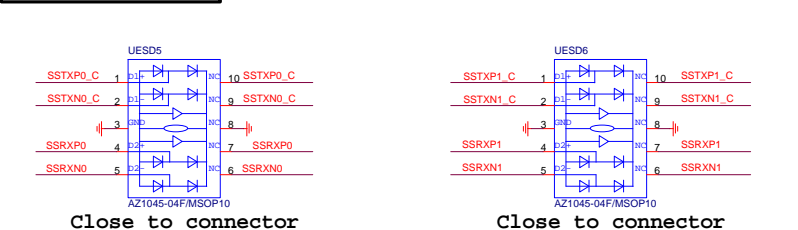


SATA_LED

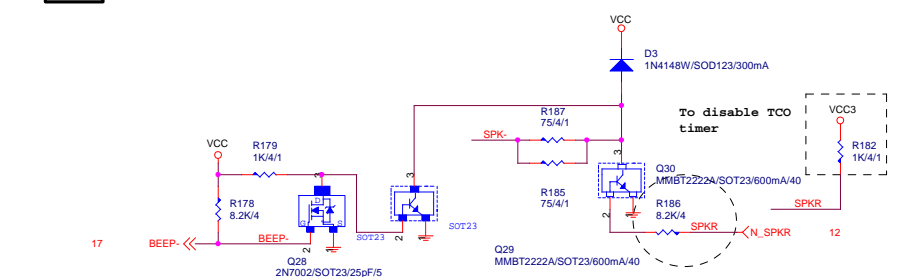


USB30_20 ESD PROTECT

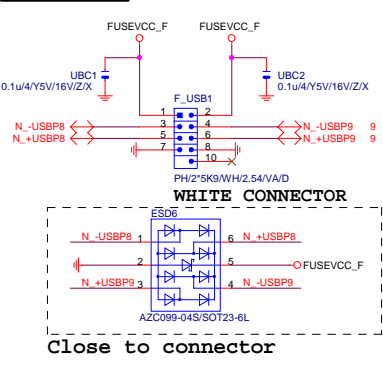
USB3.0 ESD



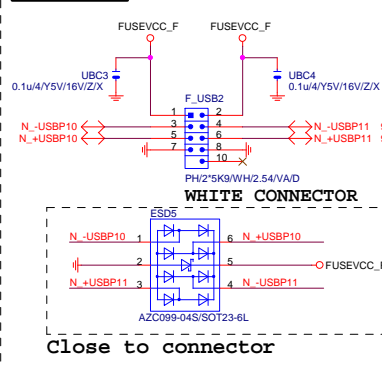
SPKR



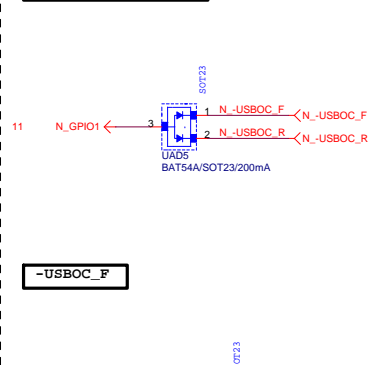
FRONT USB1



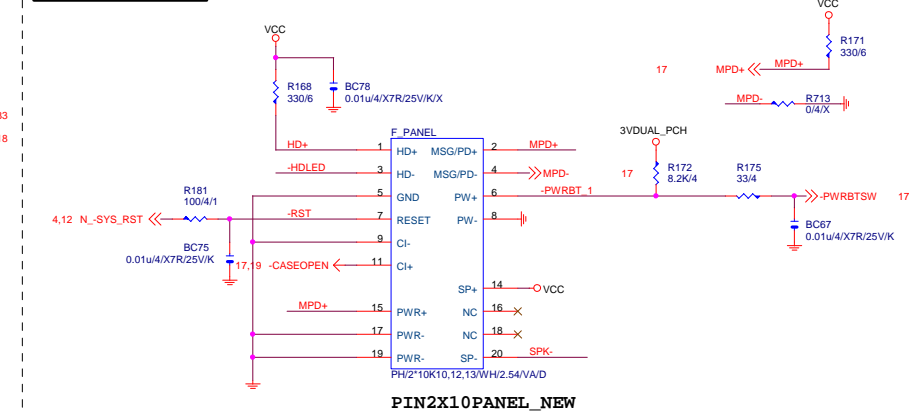
FRONT USB2



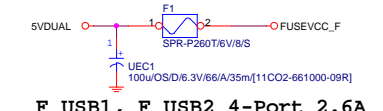
USB POWER PROTECT



INTEL FRONT PANEL

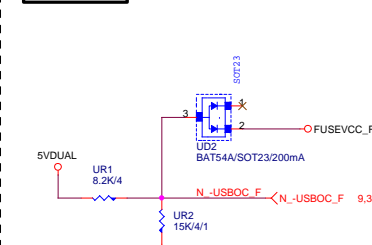


FUSE-0805



F_USB1, F_USB2 4-Port 2.6A

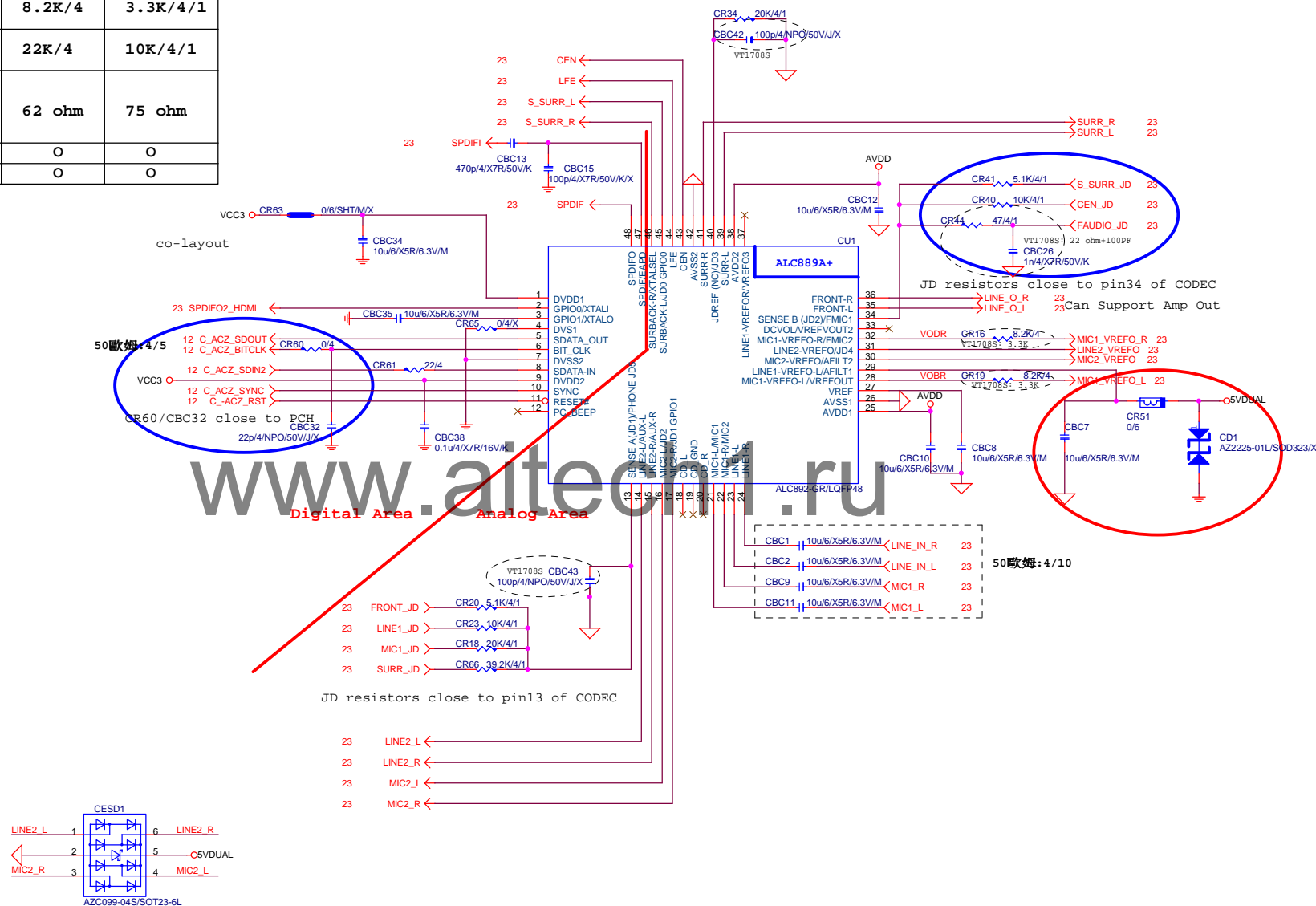
-USBOC_F



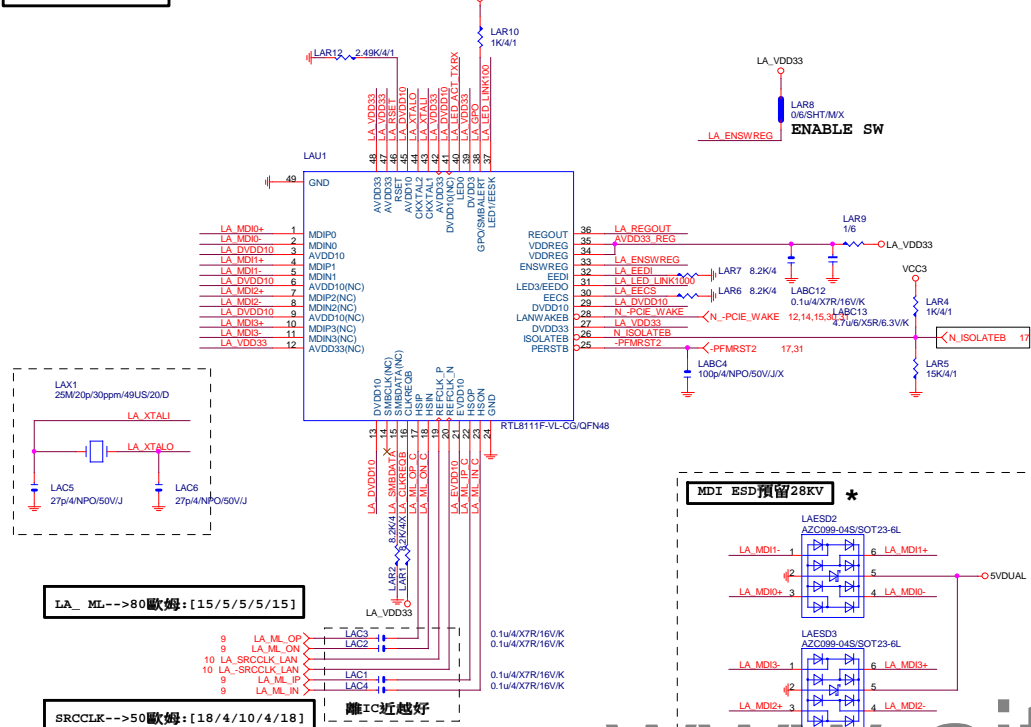
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Gigabyte Technology			
FP.F_USB_USB PWR.SPKR.SATA_LED			
GA-H81M-HD3			
Rev	1.01		
Date:	Friday, September 13, 2013		
Sheet	21	of 33	

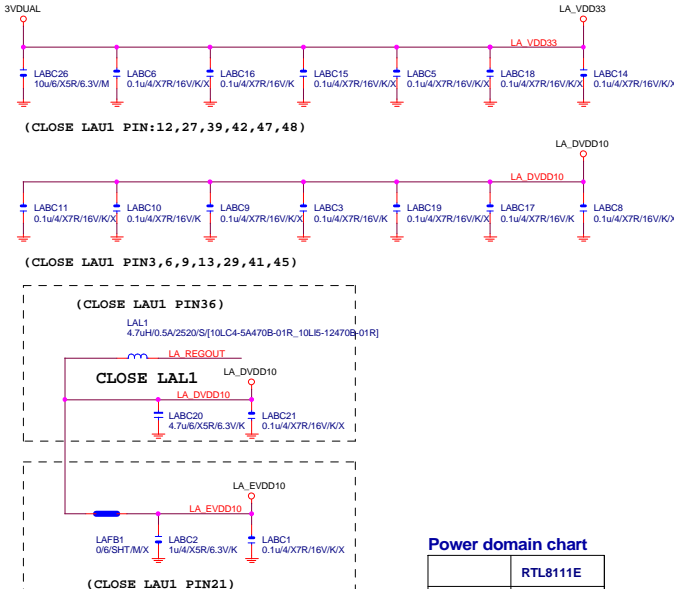
	ALC892	ALC887-VD2	VT1708S-CE
CR44/CBC26	47ohm+1nF	47ohm+1nF	22ohm+100P
CBC42/CBC43	X	X	100P/4
CR16/CR19 CR52/CR56/CR10/CR9	8.2K/4	8.2K/4	3.3K/4/1
CR6/CR7/CR58/CR54/ CR67/CR68/CR69/CR70	22K/4	22K/4	10K/4/1
CR5/CR8/CR1/CR14/ CR17/CR22/CR73/CR74/ CR13/CR11/CR57/CR53/ CR75/CR76	62 ohm	62 ohm	75 ohm
CR51/CD1/CBC7	O	O	O
CESD1	O	O	O



LAN:RTL8111F/VB/VL



LAN POWER

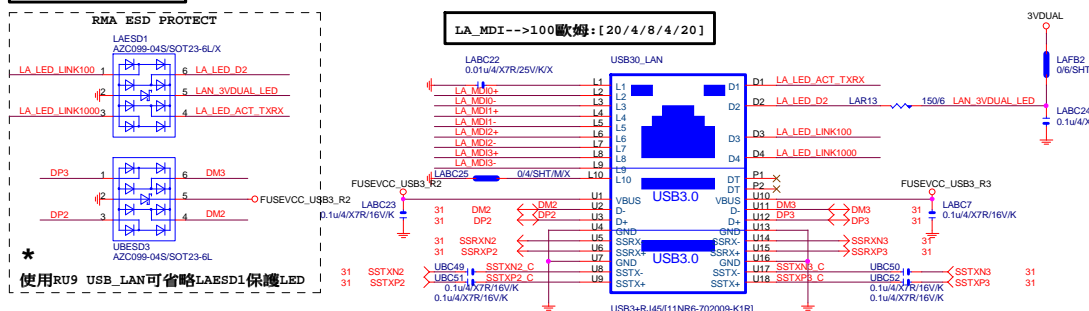


Power domain chart

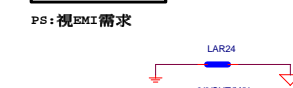
Power Domain	Voltage
AVDD33	3.3V
DVDD33	3.3V
VDDREG	3.3V
DVDD10	1.05V

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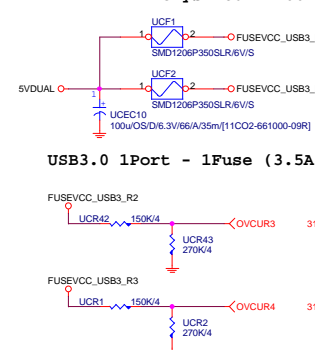
USB_LAN CONNECTOR



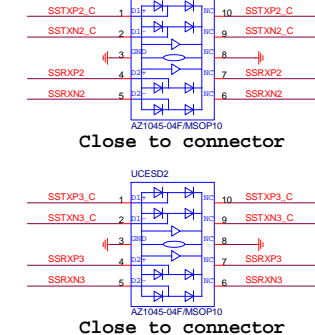
EMI SHORT PAD



Polyswitch-1206



Close to connector

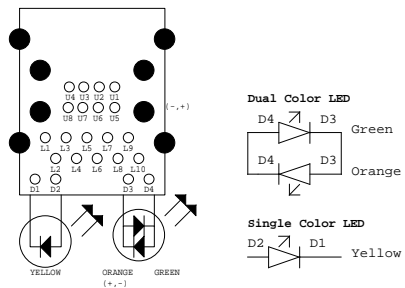


注意:USB PORT(目前:暫代6,7PORT)
USB-->90歐姆:[15/4.5/7.5/4.5/15]

BOM NOTICE

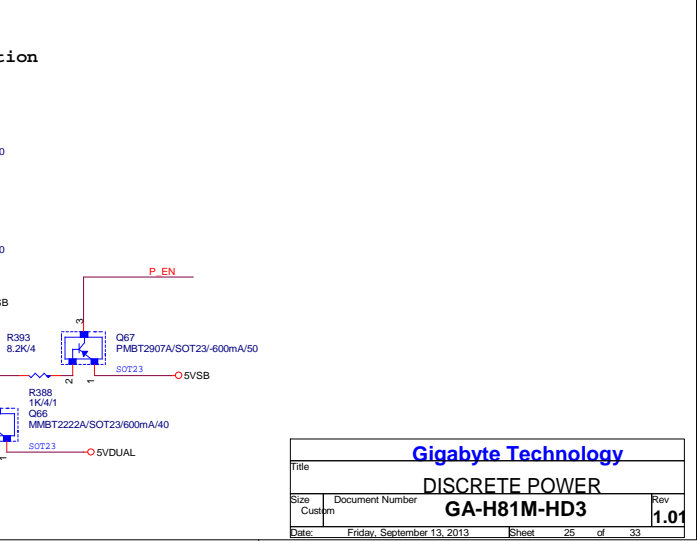
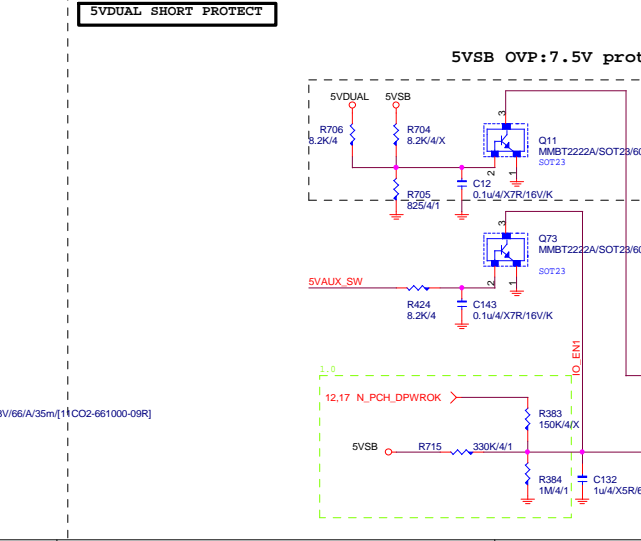
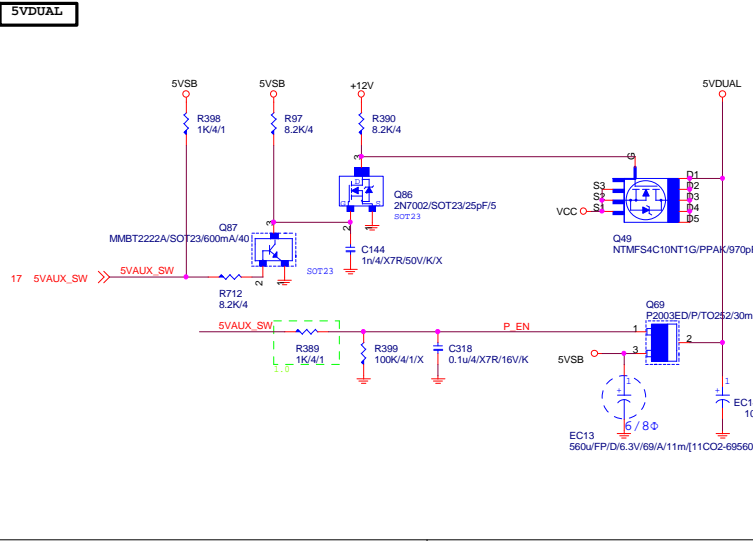
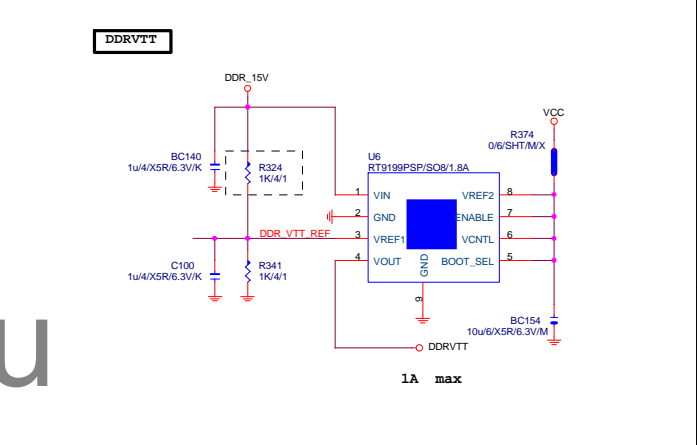
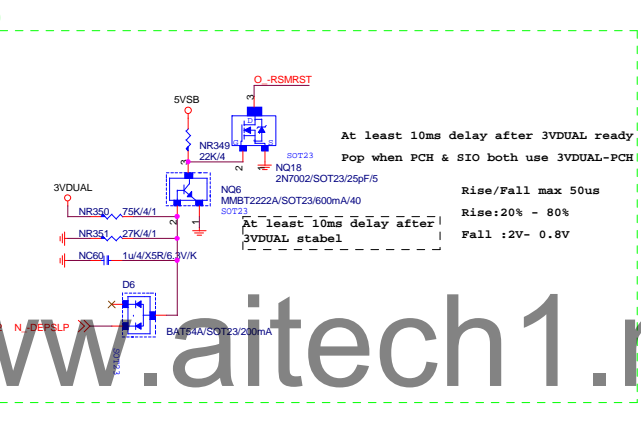
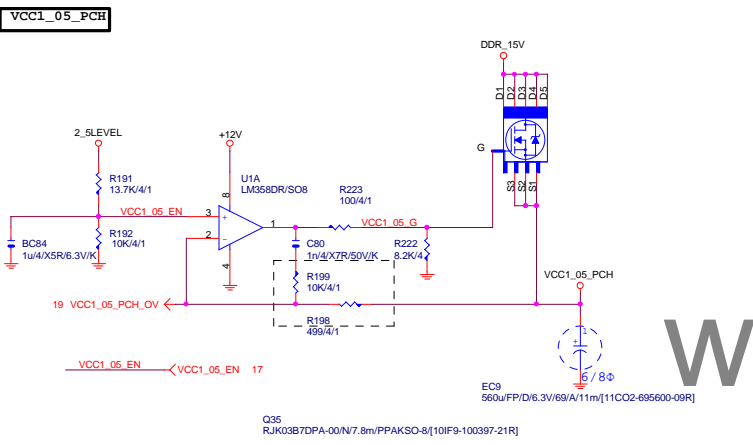
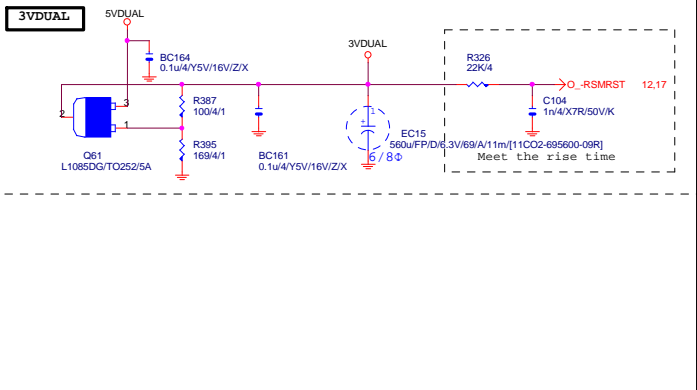
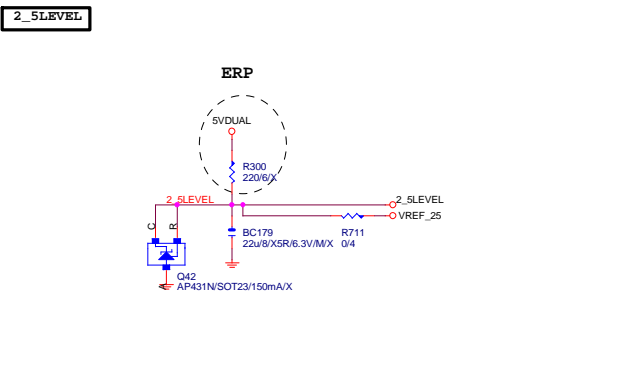
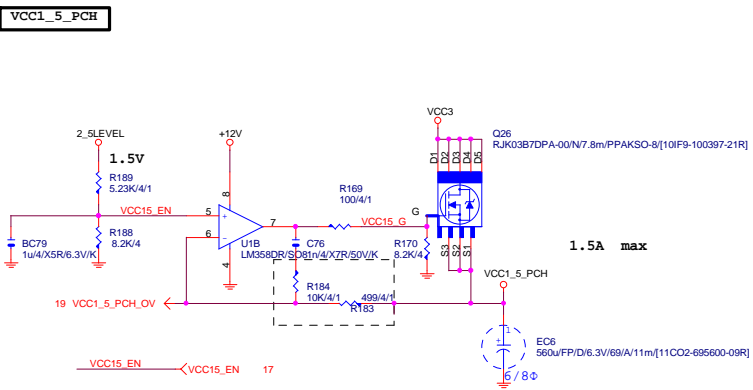
料號	規格	廠商
11NR6-702009-96R 1G LAN (12core)	UDE(RU9 ESD+)	LAESD1
[LED獨立走線,可省略外加AZC099料件LAESD1]		

- 9KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
- 28KV ESD BOM:
USB_LAN (RU9):11NR6-702009-96R
LAESD2,LAESD3:上件AZC398-04S



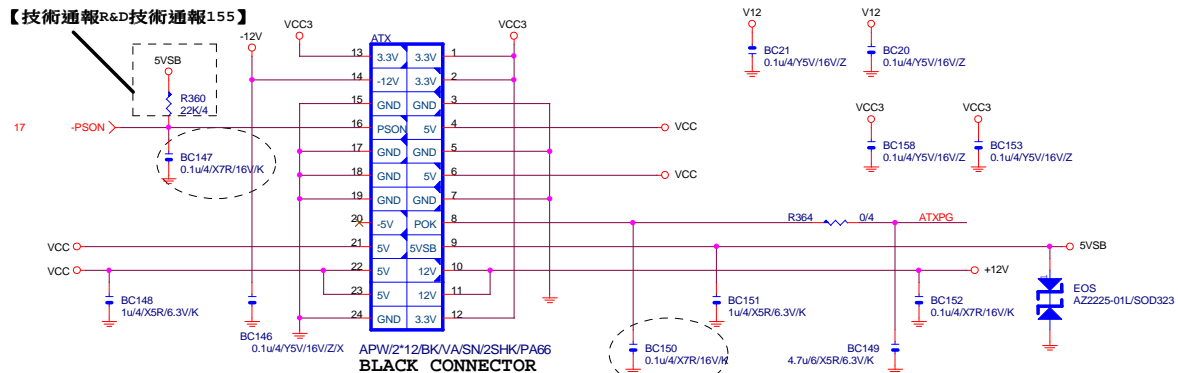
Gigabyte Technology

Title	Realtek RTL8111G
Size	Document Number
Custom	GA-H81M-HD3
Date	Rev
Friday, September 13, 2013	1.0

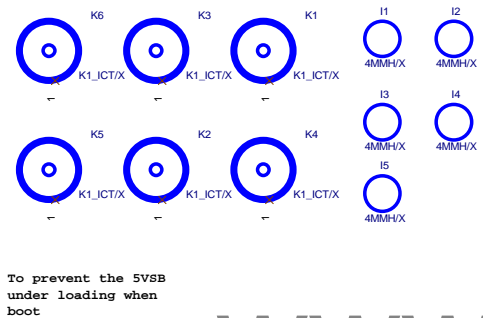
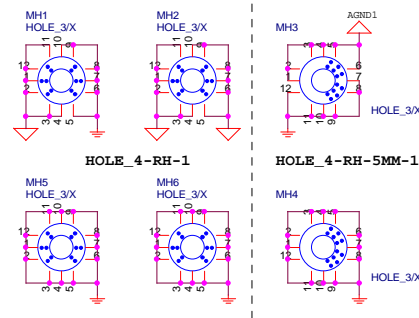
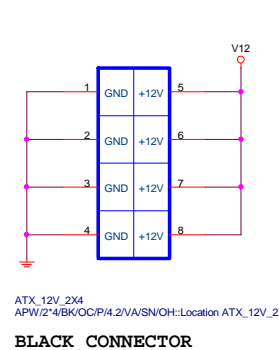


ATXX24 POWER CONNECTOR

【技術通報R&D技術通報155】



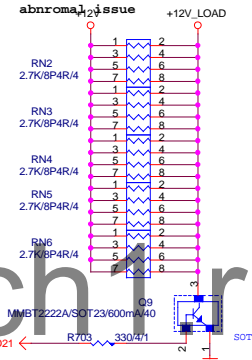
ATXX4 POWER CONNECTOR



To prevent the 5VSB under loading when boot

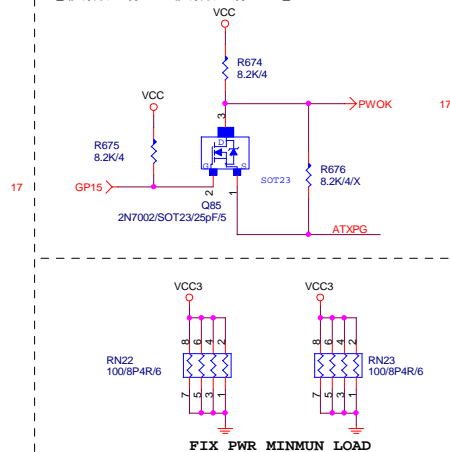
【技術通報R&D技術通報153】

To fix 12V light load abnormal issue



PWOK PATCH

【技術通報R&D技術通報154】



Gigabyte Technology

ATX CONNECTOR

GA-H81M-HD3

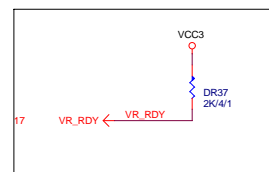
Rev 1.01

Date: Friday, September 13, 2013 Sheet 26 of 33

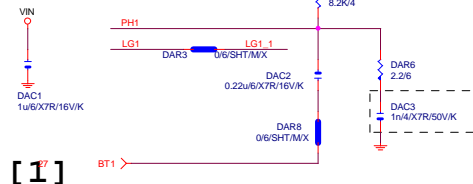
R_PROG1 (Kohm)	3-Phase Iccmax(A)
24.9	105
28.7	114
34.0	129
42.2	144

R_PROG2 (Kohm)	Fsw(KHz)	VBOOT
64.9	315	1.75
73.2	315	1.70
80.6	315	1.65
90.9	315	0

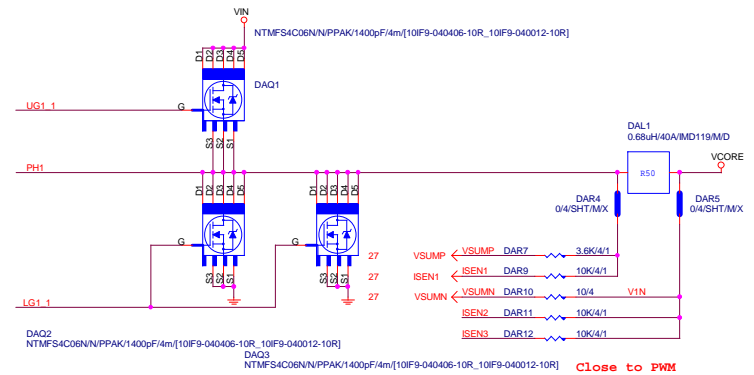
R_PROG3 (Kohm)	Fast Slew Rate (mV/us)
3.24	12
5.76	24
9.31	40
13.3	45



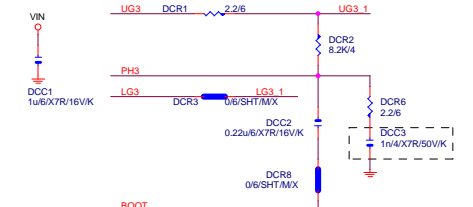
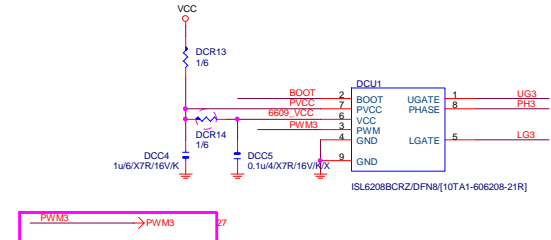
PHASE 1



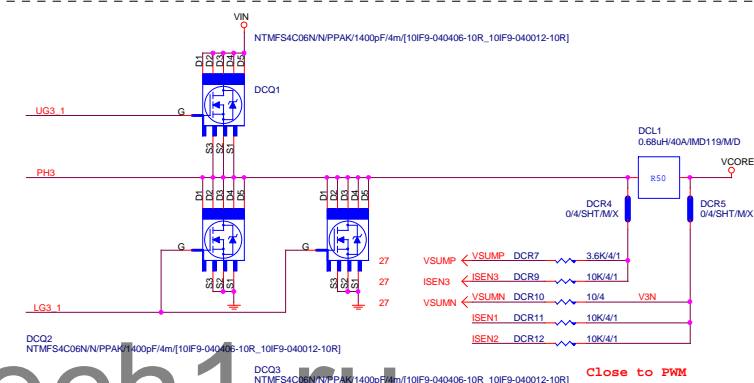
[1]



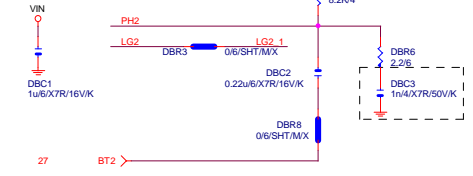
PHASE 3



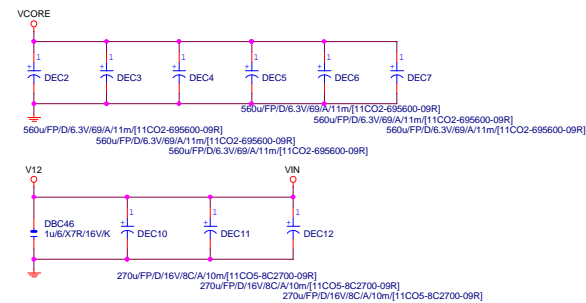
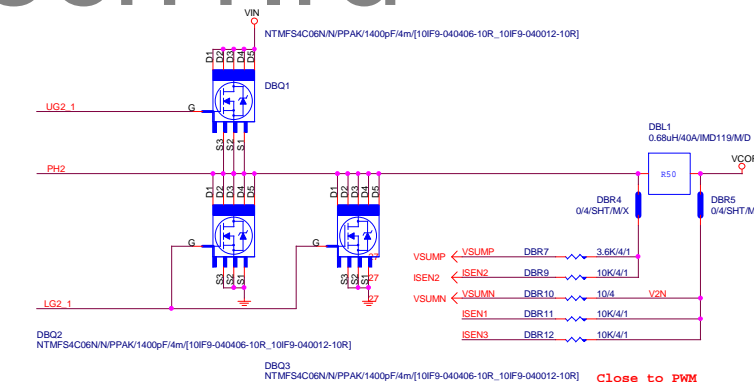
[3]



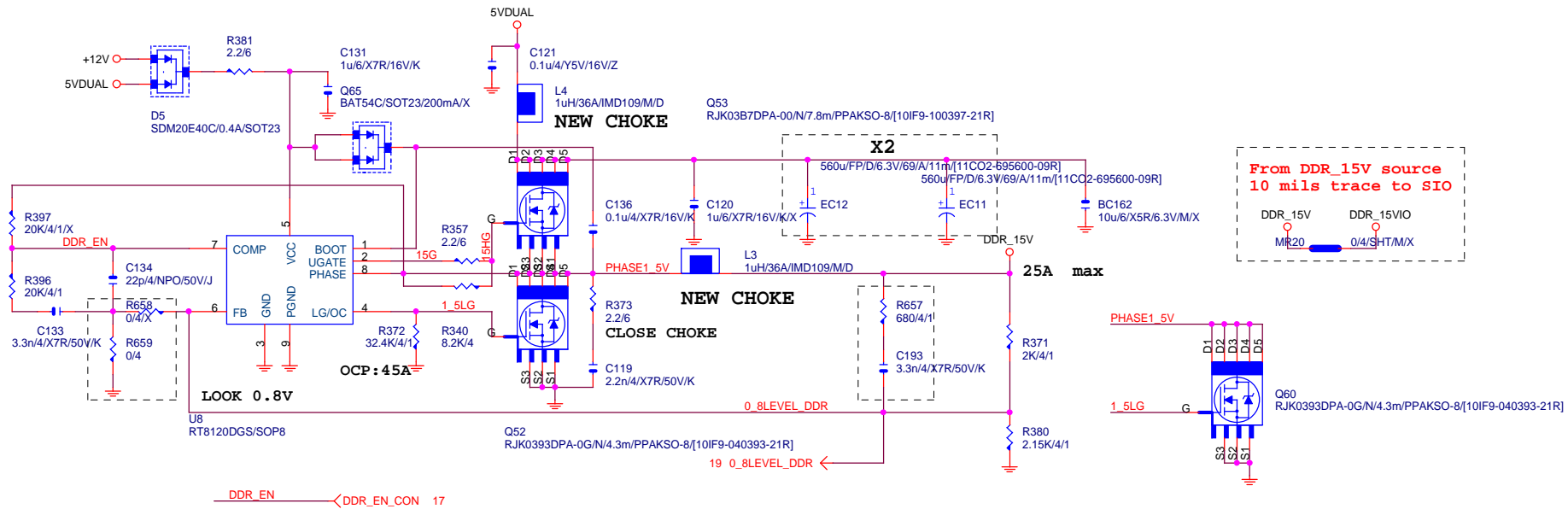
PHASE 2



[2]



DDR15V



PWR_SEQ

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VIN=5V, VOUT=1.5V, IOU=25A, PHASE=1
 IRMS=11.45A
 560u/FP/D/6.3V/68/8m RIPPLE CURRENT=4.7A
 Coefficient=1.7(85°C), 1(105°C)
 VIN Ripple current=4.7X1.7=7.99A(85°C)
 -->故固態電容須2X7.99=15.98>11.45A

$Rocset = (I_{ocp} * L_{gate, rdson}) / I_{ocset}$
 $Rocset = (45A * 6.7m\Omega) / 10uA = 30K$
 $I_{ocset} = 10uA$

Gigabyte Technology

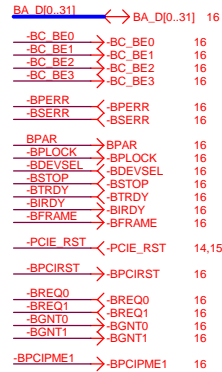
RT8120_DDR POWER

Size	Document Number	Rev
Custom	GA-H81M-HD3	1.01

Date: Friday, September 13, 2013 Sheet 29 of 33

PCIE TO PCI

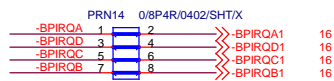
PCI:5/4/5 Impedance=50 +- 15%



```
High: Enable PCI CLK 66MHz
Low: Disable PCI CLK 66MHz
```



High: PCICLK INPUT form CLK Gen
Low: PCICLK OUTPUT form IT8893 chip



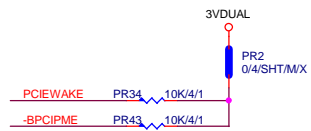
PCI slot



PCI slot

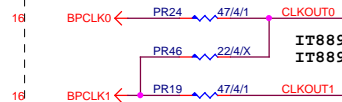


chipset side

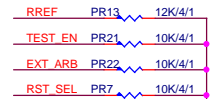


Co-Lay IT8893 (IT8893 CLKOUT1 N/A)

```
IT8892: PR24 -> 47ohm
IT8893: PR24 -> 22ohm
```



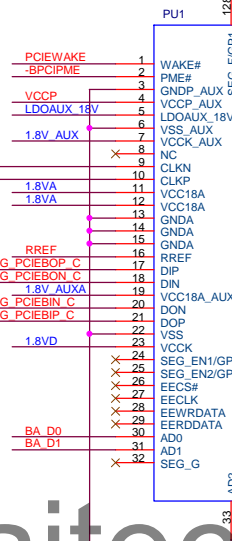
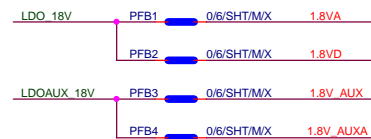
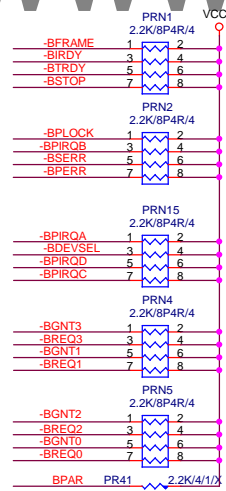
```
IT8892: PR19 -> O
IT8893: PR19 -> X
```



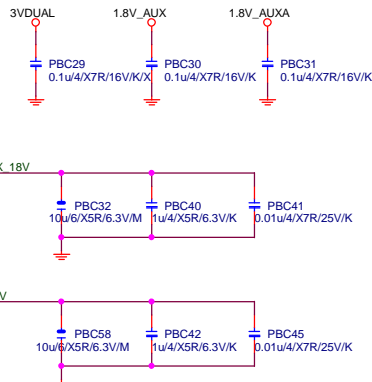
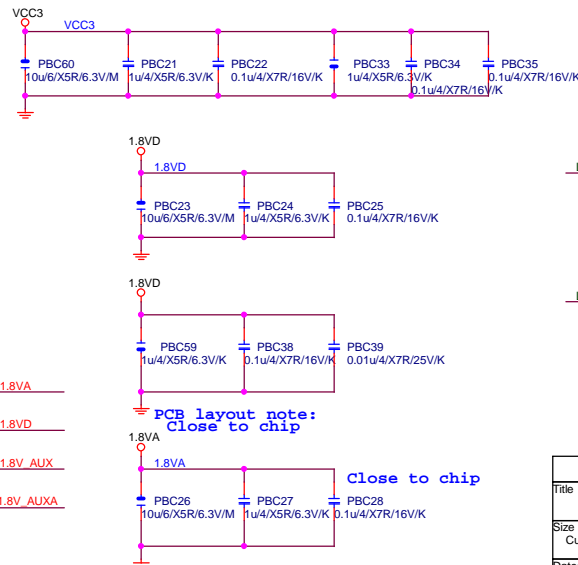
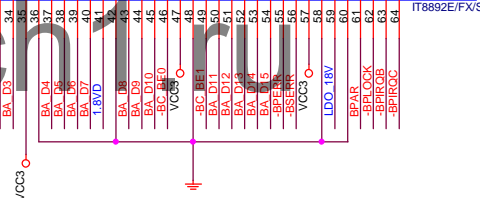
10 G_-PBCLK >

9 G_PCIEBOP PBC61
9 G_PCIEBON PBC62

9 G_PCIEBIN PBC43
9 G_PCIEBIP PBC44



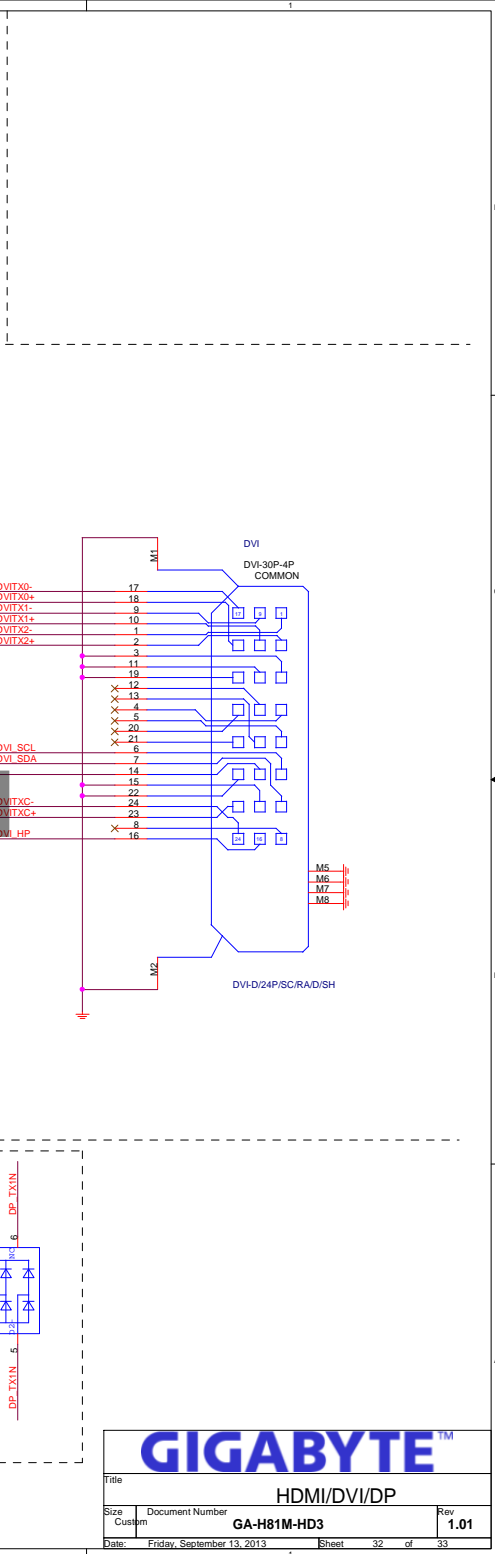
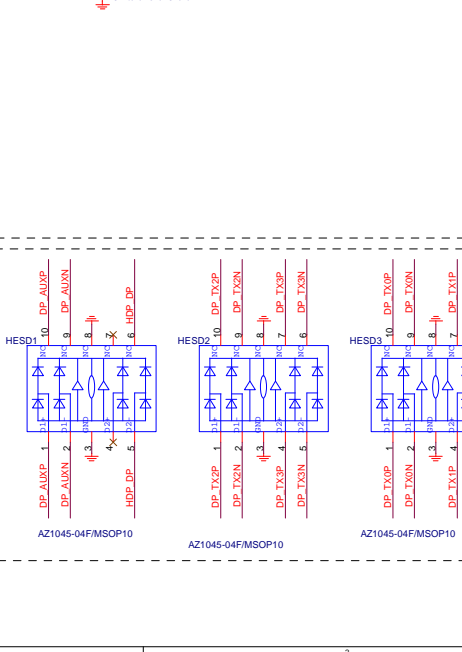
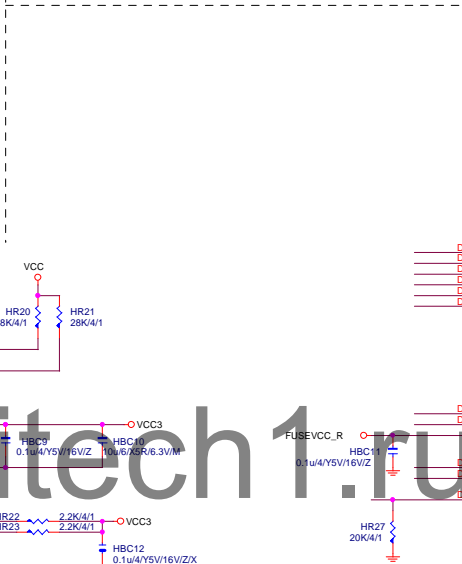
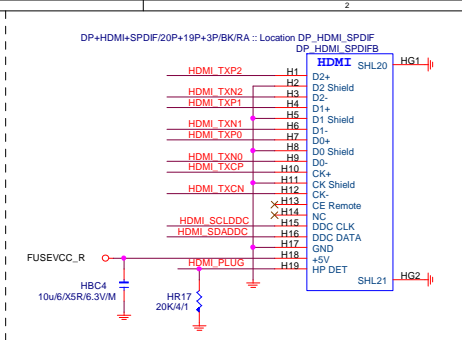
IT8892E/BX LQFP128



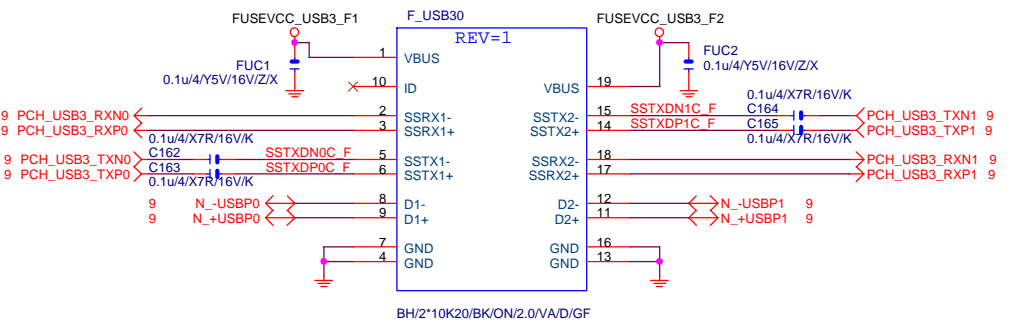
PCB layout note:
Close to chip

Gigabyte Technology

Title			
ITE IT8892E			
Size	Document Number		Rev
Custom	GA-H81M-HD3		1.0
Date: Friday, September 13, 2013		Sheet 30 of 33	

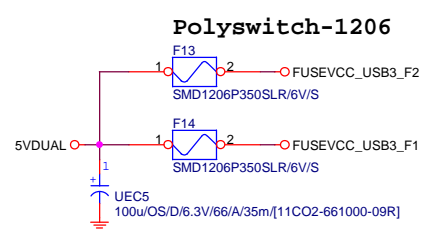


F_USB30

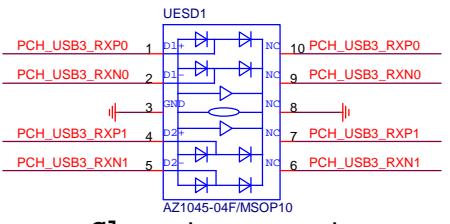


BLACK CONNECTOR

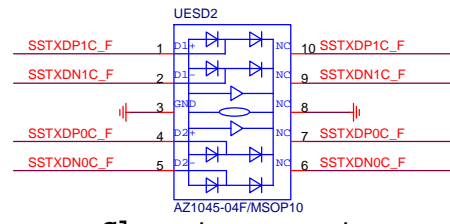
F_USB30 PWR



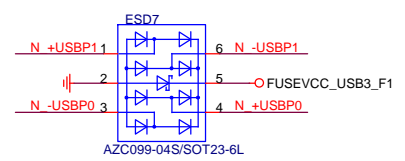
USB3.0 1Port - 1Fuse (3.5A)



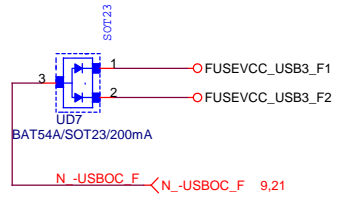
Close to connector



Close to connector



Close to connector



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